National University of Tainan

Graduate Institute of Mechatronic System Engineering

2009 spring Industry Research Master Program in Precision Industry

Master dissertation

Optimal residual stress in the CMOS fabrication

Student: Ngo Bao Quyen

Advisor: David. T.W. Lin

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Optimal residual stress in the CMOS fabrication

by

Ngo Bao Quyen

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Master Dissertation

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論文題目：Optimal residual stress in the CMOS fabrication

指導教授：David T.W. Lin

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ABSTRACT

Residual stress characterization in micro-electro-mechanical systems (MEMS) structures is of inherent importance in various respects. From the device perspective, the existence of residual stress essentially changes the performance and reduces the structural integrity and longevity of MEMS devices. Within the thesis, the specific method is proposed by using ANSYS with two main purposes. First, a finite element simulation model has been developed for a bridge structure with residual stress to predict the induced elastic deformations and stresses distribution within the structure. The simulation results about the pre-deformation caused by residual stress agree well with experimental data and the deviation is suitable with criteria. Second, the “birth and death” method is used on the analysis of the residual stresses during the CMOS fabrication process. The validated results for the fabrication process are obtained from the comparison between the simulated results and previous study. This means that the proposed method can simulate the real model effectively. In this thesis, an optimal method is used for reducing residual stress in CMOS fabrication. It uses the finite element

method combined with the simplified conjugated gradient method (SCGM) to find the minimization of Von Mises stress in CMOS fabrication.

Keywords: Residual stress, CMOS fabrication, birth and death method.

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CONTENTS

TABLE CAPTIONS

FIGURE CAPTIONS

NOMENCLATURE

σ	[Pa]	Residual stress
σ_0	[Pa]	Normal stress
σ_1	[Pa]	Gradient stress
M	[N.m]	Equivalent bending moment
I	[Kg.m^2]	Moment of inertia of cross – section
L	[m]	Length of micro – cantilever
ρ	[m]	Radius of curvature
x, y	[m]	Location
h	[m]	Thickness of film layer
σ_q	[Pa]	Quenching stress
σ_{tc}	[Pa]	Thermal stress
α	[–]	Coefficient of thermal expansion
T_i	[K]	Temperature
E	[Pa]	Young's modulus
ν	[–]	Poison ratio
S_x, S_y, S_z	[Pa]	Stress follow x, y, z direction respectively

1. OVERVIEW

1-1 MEMS overview

In recent, the Micro – Electro – Mechanical Systems (MEMS) concept has grown to encompass many other types of small things, including thermal, magnetic, fluidic, and optical devices and systems, with or without moving part. The choice of materials in MEMS is determined by micro-fabrication constraints. Integrated circuits are formed with various conductors and insulators that can be deposited and patterned with high precision. Most of these are inorganic materials (silicon, silicon dioxide, silicon nitride, aluminum, and tungsten), although certain polymers are used as well. The range of materials has now become very broad and many of these are used in thin-film form. MEMS devices are fabricated with a variety of method. Two principal micro fabrication processes for micro-structures are: (1) adding materials to the substrate by deposition processes and (2) removing material of the substrate by etching processes. The fabrication process is main reason generates residual stress in MEMS devices.

1-2 Residual stress in MEMS devices

Residual stress characterization in Micro – Electro – Mechanical Systems (MEMS) structures is of inherent importance in various respects. The existence of residual stress essentially changes the performance and reduces the structural integrity and longevity of MEMS devices. As the result, in recent years there has been rapid growth in the field of MEMS residual stress characterization. For MEMS, the existence of residual stresses can seriously influence the reliability and dynamical characteristics of devices. From the structural integrity perspective, one must predetermine or control the residual stress level to prevent structural failures and for mechanical design. So, the mechanical properties of MEMS

materials should be characterized. The existence of tensile residual stress in thin – film structures usually results in cracking of the film. On the other hand, the existence of residual stress could also effectively change the effective stiffness of structures and, therefore, the system dynamical parameters such as natural frequencies, which must be accurately determined for devices performance prediction. An accurate characterization of the state of residual stress is essential for the success of such devices.

Residual stress can be defined as those stresses that remain in a material of structure after manufacturing and processing, in the absence of external forces. It's important to note that the residual stresses are deduced using material parameters such as Young's modulus and Poison ratio together with an appropriate mechanical constitutive model. The origins of residual stresses may be classified as mechanical, thermal. Mechanically generated residual stresses are often a result of manufacturing processes that produce non – uniform elastic or plastic deformation. On the other hand, thermally generated residual stresses are not only the consequence of non – uniform heating or cooling but also are developed in material during fabrication and processes as a consequence of the Coefficient of Thermal Expansion (CTE) mismatch between different phases or constituents.

1-3 Case study

Nowadays, the finite element method (FEM) is a powerful tool to predicting the phenomena of engineering system. It enables engineers and designers to create virtual prototypes of their designs operating under the realistic operating conditions and provides to the analysis industry. Along with experimental method, FEM is an extremely important factor in development MEMS field. In this thesis, ANSYS software is used to simulate the residual stress in two situations: First, demonstrate the effect of residual stress to bridge structure. A finite element simulation model is used to simulate the effect of residual stresses in the bridge

structure under the normal and gradient stress. Second, investigate into the development of the residual stresses in CMOS fabrication process. The optimal method (SCGM) is used to reduce residual stress. Through two cases, it is clearly to see that the effect of residual stress in MEMS industry, about the deformation, stress distribution… in MEMS field. On other hand, we not only find the factor causing residual stress but also reduce residual stress in MEMS by optimal method.

2. THE RESIDUAL STRESS INDUCED ELASTIC DEFORMATION OF MICRO STRUCTURE BY STANDARD CMOS PROCESS

2-1 Introduction

In the decades since electronic thin-film fabrication techniques were first used to produce microelectromechanical system (MEMS), significant progress has been made in modifying MEMS manufacturing processes to reduce film stresses and stress gradients. As a result of this progress, out-of-plane deformation of free standing micromachined films can be limited to a level sufficient for many types of electromechanical sensors and actuators.

A principal source of contour errors in micromachined structures is residual strain that results from thin-film fabrication and structural release. Both processes impose residual stresses in fabricated thin films. When sacrificial layers of the device are dissolved, residual stresses in the elastic structural layers are partially relieved by deformation of the structural layers. The extent of deformation is strongly dependent on process details and on the structure's geometry. Stress gradients through the thickness of a thin film are particularly troublesome because they can cause significant curvature of a free-standing thin-film structure even when the average stress through the thickness of the film is zero.

Micro – beams are very popular in MEMS product and widely used in many applications. Three kinds of effect resulted from the stress will affect the behavior of beam. The first is non-uniform stress, and it will cause the curling of cantilever beam. The second effect is the nonlinear spring effect result from bending stiffness in the doubly-supported beam. The last is the compressive residual stress, and it will result in the buckling of the beam. In this thesis, a

fixed-fixed beam structure is proposed as a test structure to demonstrate the deformation under the residual stress effect. There are two kinds of the residual stress inside the thin film of fixed-fixed beam structure. Normal stress is the average compressive stress and gradient stress is resulted from the deposition. Once the beam is released, the beam length increases slightly, relieving the compressive stress so that the average stress goes to zero but the gradient stress still presents. The gradient stress creates the original stress-gradient-imposed external bending moment transferred into the internal bending moment to bend the beam. At the time of beam bending, it decreases the tensile stress at the top of the beam and the compressive stress at the bottom of the beam. The stress created by bending varies linearly through the axis of the beam thickness. For the case of an initial linear residual gradient stress, the stress variations created by bending exactly will equivalent the initial stress variation.

Base on the above cited phenomena, we use the finite element method (FEM) to simulate the deformation of the 2P2M bridge structure under the residual stress consideration (normal stress and gradient stress). The new detective method is proposed and compared with experimental data. After that, we can obtain the relationship between the length/width of bridge and deformation to design the stable MEMS products in advance.

2-2 Literature review

Microelectromechanical system (MEMS) devices commonly employ freestanding structures which are suspended with underlying air-gap, but mechanically fixed on substrates by one or more anchors [1]. An inherent problem of freestanding structures is out-of-plane deformation, causing an alteration in designed value of air-gap thickness, induced by residual stress of the deposited films. The deformation of MEMS structure usually results in a deterioration of device performance, therefore its control is a critical issue in developing many sensors and actuators.

The deformation profile depends on stress state and geometry of MEMS structure. There is vast literature on topic relating to the residual stress and the resultant elastic deformation. In 1999, Fang et al. proposes a buckling of bridge (fixed-fixed beam) is generated by only compressive stress [2], while a bending of cantilever (fixed – free beam) is by both tensile and compressive stresses [3]. The bending profile of cantilever is analyzed to curvature components induced by mean and gradient stress, respectively [3]. Fang and Wickert [4], Greek and Chitica [5] studied the monolayer cantilever with linearly gradient residual stress. Hubbard and Wylde [6] presented a discussion on the monolayer cantilever with arbitrarily distributed residual stress.

In the other hand, the deformation caused by the residual stresses play an important role in the development of MEMS products [1]. Therefore, the relationship between the residual stress and curvature in thin-film structures is an active area of research, both for the development of MEMS technology and for the fundamental science of film growth. For bilayer structures, the first formula contributed by Stoney provides an approximate expression for the curvature of a film-substrate structure in terms of uniform residual stress in the film [7]. Other approximated solutions include expressions by Brenner and Senderoff [8]. For

multilayered structures, a closed-form solution was first presented by Townsend et al. [9] and then improved by Klein and Miller [10]. Besides, Huang and Zhang [11] extend the Stoney formula for a film–substrate system with a gradient residual stress in the film and also presented two approaches to relate the arbitrarily distributed residual stress to the resultant elastic deformation of multilayered MEMS structures [12].

In the addition, the mechanical properties of thin film material are very necessary on the evaluation of the elastic deformation caused by the residual stresses [12]. Petersen and Guarnieri [13] propose Young's modulus measurement of thin films using micromechanics. Vlassak and Nix [14] study new bulge test technique for the determination of Young's modulus and Poisson's ratio of thin films. Chudoba et al. [15] and Riester et al. [16] focus on the shear modulus and residual strain measurement, respectively. Gupta [17] study residual stress of thin films in MEMS. If Young's modulus of thin film material is known, mean and gradient stresses can be quantitatively extracted from the deflection profile of single-layered bridge or cantilever by numerical modeling based on finite element method [18]. But, real MEMS devices mostly have multilayered structures with different materials and complex geometries, therefore the modeling of their deformations would be practically difficult to implement.

Meanwhile, many experimental methods have been developed to demonstrate the variation of the deformation under the different residual stress value. Residual stress of a single Si_3N_4 film was controlled by the deposition condition to change the curvature shape of optical filter membrane [19]. Overall stress of poly-Si multilayer was diminished by the alternate deposition of tensile and compressive layers to have an optimized ratio of relative thicknesses [20].

According the above citing references, in this thesis, the experimental method that measures the deformation of the 2P2M bridge structure by image analysis is compared with finte element method to propose a new detective method to predict the deformation of bridge structure under the residual stress effect. It is expected that this method can provide components to assist designers as a design reference and industrial development in the mass production process.

2-3 Modeling and experiment

2-3-1 The government equation of the residual stress in thin film

Thin films deposited onto substrates will result in the residual stresses. Non – uniform residual stresses in the cantilevers, due either to a gradient stress through the cantilever thickness or to the deposition of different material onto a structure, can cause the cantilevers to curl and profound the effects on the mechanical behavior of devices. Therefore, the residual stress is expressed as [21]

$$\sigma = \sum_{k=0}^{\infty} \sigma_k \left(\frac{y}{h}\right)^k \approx \sigma_o + \sigma_1 \left(\frac{y}{h}\right) \tag{2.1}$$

where σ: Residual stress; σ_0: Normal stress; and σ_1: Gradient stress. The schematic diagram of the stresses described in Fig. 1.

2-3-2 A finite element simulation model of the bridge structure

The bridge structure includes many thin film layers deposited on the silicon substrate. Fig. 2 shows the SEM picture of the bridge structure fabricated by Macronix International Co. (MXIC) 2P2M process [22]. Illustration of the bridge structure is shown in Figs. 3(a)-(b) in detail. The thickness of each layer and its material characteristic is given in table 1. To evaluate the deformation distribution of the bridge structure resulted from residual stress, a finite element model is developed using ANSYS 11. PLANE183 is described in Fig. 4 [23] is selected for the analyses. This element is defined by 8-nodes or 6-nodes having two degrees of freedom at each node. The element may be used as a plane element (plane stress, plane strain and generalized plane strain) or as an axisymmetric element. Specially, the stress use as load is supported. For the bridge structure, components are only a few microns in size, so this model uses the conversion factors from standard MKS to μMKSV. Fig. 5 demonstrates the

bridge structure in ANSYS. In micro - system technology, the approximate thickness of substrate (400µm ~ 675µm) due to the deposited layer thickness is about 20µm to result in the extreme fine meshing. The FE mesh model is constructed into 2 parts. First, the quadrilateral mesh is used in the film layer except substrate, element size is 0.1 x 0.1µm^2. Second, the free mesh is used in the substrate, the size of element is 0.3 x 0.3µm^2. The mesh models are shown in Fig. 6.

A symmetric model is employed to reduce the solving time. Only half of the bridge structure is modeled using the symmetry boundary condition, described in Fig. 5. The displacement along the line of the symmetry is confined ($U_x = 0$), the nodes at the bottom is confined in all direction ($U_x = 0$, $U_y = 0$) to prevent a rigid body motion. The residual stress inside the bridge structure results in the bridge deformation. The value of residual stress is given by table 2.

2-3-3 Simulation methodology

We recall from the previous section that the residual stresses in the beam include: (1) normal stress – constant through thickness of film, (2) gradient stress – variation through thickness of the thin film. Fig. 7 demonstrates clearly the distribution of the residual stress in one thin film in FE method. The deformation will appear after the residual stress releases. Another section in developing the MEMS product, the deformation of MEMS product which the specific value of the residual stress to guarantee the stability of the product is an important issue. That's why choosing material in the MEMS field plays the key role. To solve that problem, it is necessary to know the effect of the residual stress in the MEMS product. In this study, the purpose is to obtain the effect of the residual stress through the deformation effectively. In general, we can only apply the constant stress at the element. Thus, if the gradient stress inside the beam will be approximated, the stress will be changed at each

element to fit the profile of the gradient stress. Therefore, more elements are better approximation of the residual stress. Fig. 8 shows the approximation of the gradient stress in detail.

Fig. 9 demonstrates the methodology for analysis effect of the bridge structure with residual stress. The comparison between the experimental and simulation will play the key role in this method. We discuss the deviation between the experiment and the simulation for the validation of this proposed methodology. After that, the parameter (length of the bridge structure, width of the bridge structure) will be changed to find the factor of the residual stress.

The equivalent stress of each film is the sum of the normal stress and the gradient stress as the Eq.(2.1) and shown in the Fig. 1. We follow the approximation of the stress illustrated as before. The stress of each element is substituted to form the equivalent stress of this bridge structure. The combination of these elements in the finite element package is shown in Fig. 10.

2-3-4 Experiment

The purpose of this part is to build up an experiment for the fabrication of the bridge structure in 2P2M and the measurement of the pre-deformation after the bridge structure released residual stress.

A micro fixed-fixed beam structure is used as a test structure and the schematic is shown in Fig. 11. The test structures were fabricated by Macronix International Co. (MXIC) standard 0.5μm 2P2M process [22]. The upper electrode is metal 2 layer, and the bottom electrode is poly 1 layer. A silicon dioxide layer between the upper electrode and the bottom electrode is a sacrificial layer (Fig. 12a).The hole between the neighboring passivation layers is etching hole, results in the sacrificial layer etched by Silox Vapox III during post-processing, and release the beam to form a gap between both electrodes (Fig. 12b). This micro fixed-fixed beam can be used to measure Young's modulus and residual stress. Table 3 presents the dimensions of

two micro fixed-fixed beams and specifies the layout of the two micro test beams. The fabrication includes two steps: the standard CMOS process (MXIC 0.5μm 2P2M process) and post-processing. After the CMOS process (Fig. 12a), the test beams are released by soaking in Silox Vapox III 30 min. Fig. 2 shows the scanning electron microscopy (SEM) photographs of the micro test beam on the chip after post-processing.

We used the scanning electron microscope (SEM) system to measure the pre-deformation after the 2P2M bridge structure released residual stress. The scanning electron microscope (SEM) is a type of electron microscope that images the sample surface by scanning it with a high-energy beam of electrons. The SEM JEOL JIB-4500 Dual Beam (focus ion beam & electron beam) System in use is illustrated in Fig. 13 [24]. The deformation curve of the bridge structure is obtained from the SEM picture analysis. The image analysis method is described in Fig. 14 with x – location follows the length of the bridge structure and y – height of gap g in detail.

2-4 Result and discussion

In this study, the aim is to predict the bridge structure's pre-deformation under the residual stress. The bridge structure deformation is caused by residual stress in Poly2, M1 and M2 layer under the effect of the internal moment created by the released stress. Fig. 15(a)-(b) show the deformation of the 2P2M bridge structure before and after released residual stresses, respectively.

The residual stress is a value and depends on the fabrication process, the characteristics of material. The residual stress of each material is proposed in table 2. In this thesis, three kinds of the 2P2M bridge structure with different length are discussed. The deformation under the effect of the residual stresses is measured in the experiment and compares with the simulation. First, the 2P2M bridge structure with length of bridge L= 130μm is mentioned. In this case, the experiment measures the deformation at 9 specific positions by using the SEM picture analysis method (Fig. 14). By measuring the gap (g) before and after released residual stress in the specific positions, the deformation can be observed. The positions and the height of gap before and after released are described in table 4 in details. Fig. 16 shows the deformation's curvature of the 2P2M bridge structure (L= 130μm) in experiment. Through this figure, the 2P2M bridge structure is bending down and the maximum deformation value is 0.136μm. Fig. 17 illustrates the deformation's curvature in simulation. The bridge is also bending down and the maximum deformation value is 0.111μm at the same position in experiment. The shape of curvature is a parabolic. In addition, the simulation result is compared with experimental data. The comparison is shown in Fig. 18. It finds that the simulation result agree well with experimental data. Table 4 describes the comparison between the experiment and simulation in detail. The deviation is also calculated. The average deviation is 3.58%.

Moreover, the 2P2M bridge structure with length of bridge L = 140μm is proposed. In this bridge structure, the residual stress of each material is the same with the previous but the length of the bridge is longer. That's why the deformation is also different. In this case, the experiment measures the deformation at 8 specific positions. That is described in table 5 in details. Fig. 19 illustrates the comparison between the experiment and simulation. The deviation is calculated in table 5. The average deviation is 10.72%.

Finally, the 2P2M bridge structure with length of bridge L = 150μm is discussed. In this case, the experiment measures the deformation at 9 specific positions. That is described in table 6 in details. The comparison between the experiment and simulation is shown in Fig. 20. The deviation is calculated in table 6. The average deviation is 10.07%.

Through the above cited comparison, the phenomenon of the deformation of the bridge structure in three cases agrees well with experiment. The deformation proportions to the length of the bridge structure. Therefore, the simulation result is reliable. It means that the finite element simulation model developed in this work is correct and robust in predicting the effect of the residual stresses in the bridge structure. On the other hand, the deformation has a relationship with the length of bridge structure. The relationship between deformation and length of the bridge structure is demonstrated in Fig. 21. It's interesting to find that the relationship is linear. That helps the designer to understand the relationship between the bridge structure geometry and the residual stress. Therefore it can provide the design reference in the development MEMS product.

2-5 Conclusion

The general purpose of the present study is to predict the deformation of bridge structure under the residual stress effect. Through the finite element package and compare with the experiment, a finite element simulation model is developed. Besides, the finite element simulation model is validated by experiment according to the bridge structure fabricated MXIC 2P2M process. It finds that the simulation agrees well with experimental data and the average deviation is suitable with the criteria. It means the finite element simulation model is powerful for developing the MEMS products.

From this study, it can be concluded that the proposed method is an accurate, robust and efficient method to determine the pre-deformation caused by residual stress in CMOS-MEMS bridge structure. Therefore, this research provides components to assist designers as a design reference and industrial development in the mass production process.

Table 1: The thickness and Young's modulus of each layer [22]

Layer	Thickness(A)	Young's modulus (GPa)
Pass(Si_3N_4/SiO_2)	10000/4500	380
Metal2(Al / TiN & Ti)	9000	77
IMD(Oxide)	7000	410
Metal1(TiN / Al /TiN & Ti)	6000	77
ILD(Oxide)	7000	410
Poly2	1800	167
HTO(Oxide)	370	75
Poly1/Wsi	1250/1500	167
Si	4800000	129

Table 2: Residual stress in the 2P2M bridge structure [25]

Layer	Normal stress σ_0 (Mpa)	Gradient stress σ_1 (Mpa)
Poly2	50	-57.5
M1	-157.5	432
M2	-8	-382.6

Table 3: Dimensions of the two micro fixed-fixed beams [22]

Parameters	Values	
Length (μm)	120	150
Width (μm)	5	
Thickness (μm)	0.9	
Gap (μm)	1.437	

Table 4: Simulation and experimental data of 2P2M bridge structure with L = 130µm

Before release		After release			
X (um)	Design (um)	Experimental data (um)	Experimental data (adjust) (um)	Simulation results (um)	Deviation (%)
0	1.437	1.412	1.4198	1.437	1.21
10	1.437	1.294	1.3011	1.405	7.98
20	1.437	1.294	1.3011	1.379	5.98
40	1.437	1.294	1.3011	1.342	3.14
60	1.437	1.294	1.3011	1.326	1.91
80	1.437	1.294	1.3011	1.331	2.30
100	1.437	1.412	1.4198	1.357	-4.42
110	1.437	1.429	1.4369	1.378	-4.10
130	1.437	1.412	1.4198	1.437	1.21
		turn 6°		original gap=1.437	Average: 3.58

Table 5: Simulation and experimental data of 2P2M bridge structure with L = 140µm

Before released		After released			
X (um)	Design (um)	Experimental data (um)	Experimental data (adjust) (um)	Simulation results (um)	Deviation (%)
0	1.437	1.286	1.2931	1.437	11.13
20	1.437	1.286	1.2931	1.378	6.57
40	1.437	1.286	1.2931	1.338	3.47
60	1.437	1.143	1.1493	1.319	14.77
80	1.437	1.143	1.1493	1.319	14.77
100	1.437	1.286	1.2931	1.338	3.47
120	1.437	1.286	1.2931	1.378	6.57
140	1.437	1.143	1.1493	1.437	25.03
		turn 6°		original gap=1.437	Average: 10.72

Table 6: Simulation and experimental data of 2P2M bridge structure with L = 150µm

Before release		After release			
X (um)	Design (um)	Experimental data (um)	Experimental data (adjust) (um)	Simulation results (um)	Deviation (%)
0	1.437	1.286	1.2931	1.437	11.13
20	1.437	1.286	1.2931	1.377	6.49
40	1.437	1.286	1.2931	1.336	3.32
60	1.437	1.286	1.2931	1.313	1.54
80	1.437	1.286	1.2931	1.308	1.15
100	1.437	1.143	1.1493	1.322	15.03
120	1.437	1.286	1.2931	1.354	4.71
140	1.437	1.143	1.1493	1.405	22.25
150	1.437	1.143	1.1493	1.437	25.03
		Turn 6°		Original gap=1.437	Average: 10.07

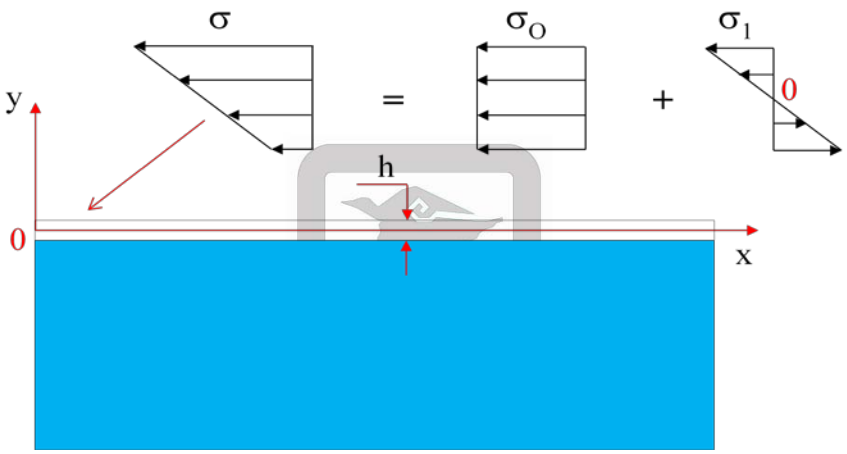


Fig. 1: Residual stress in thin film

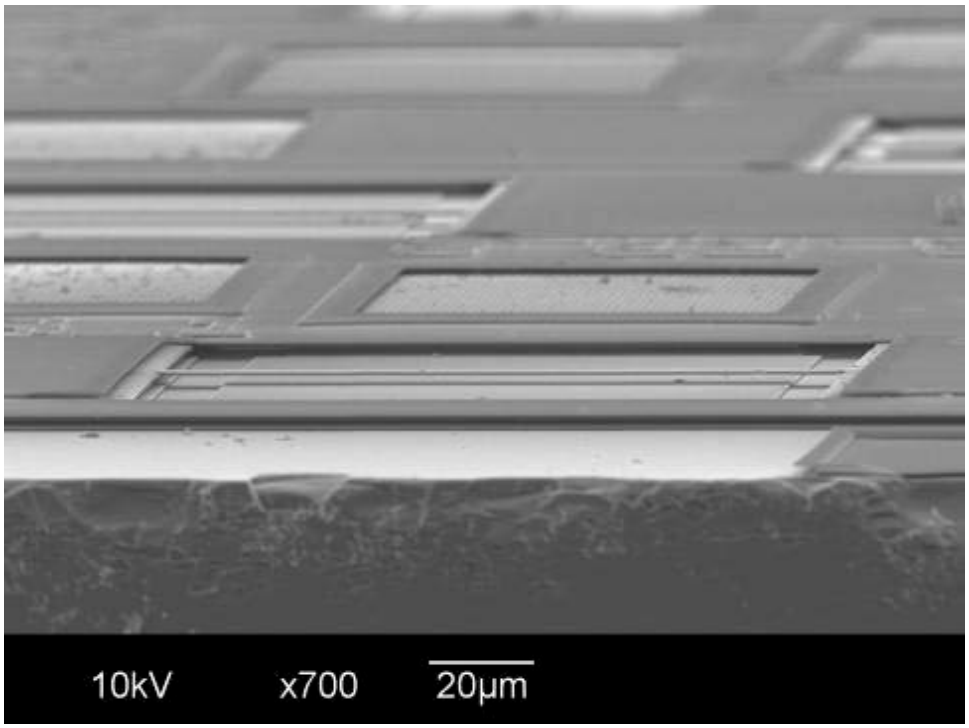
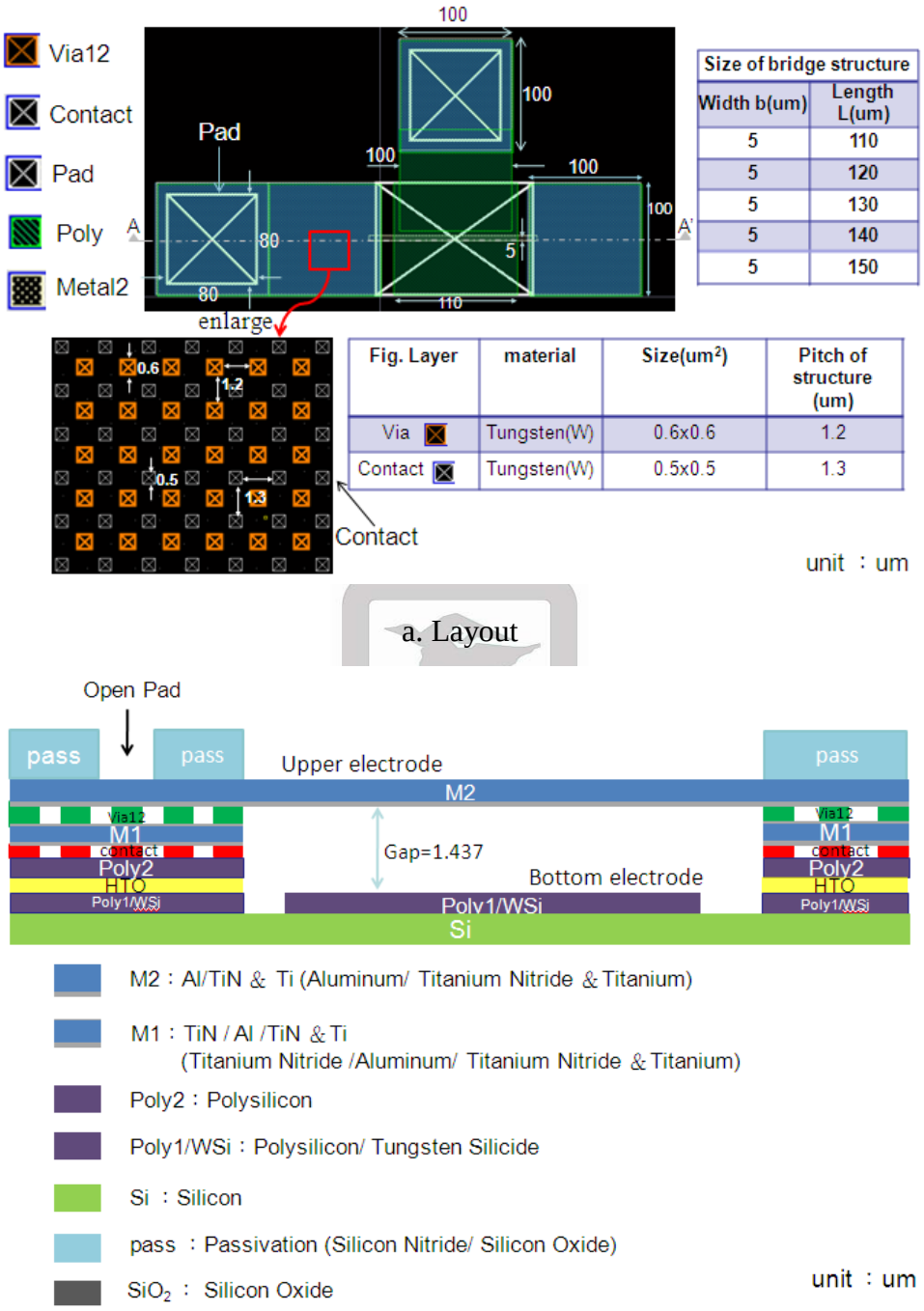


Fig. 2: SEM picture of 2P2M bridge structure [22]



a. Layout

b. Section A – A'

Fig. 3: Illustration of the bridge structure [22]

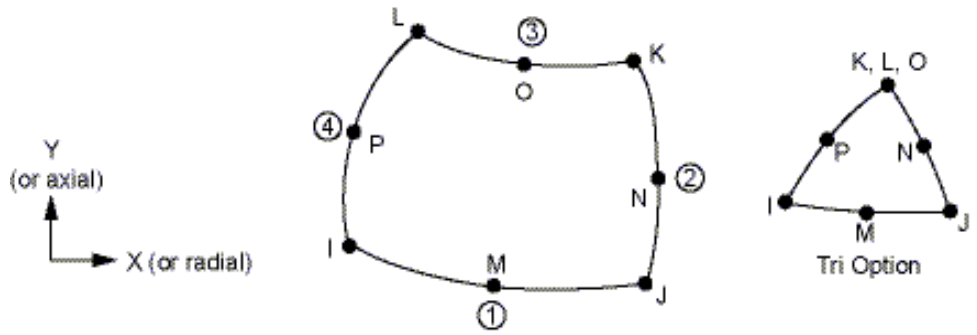


Fig. 4: The element of PLANE183 in ANSYS [23]

Fig. 5: The model of the bridge structure

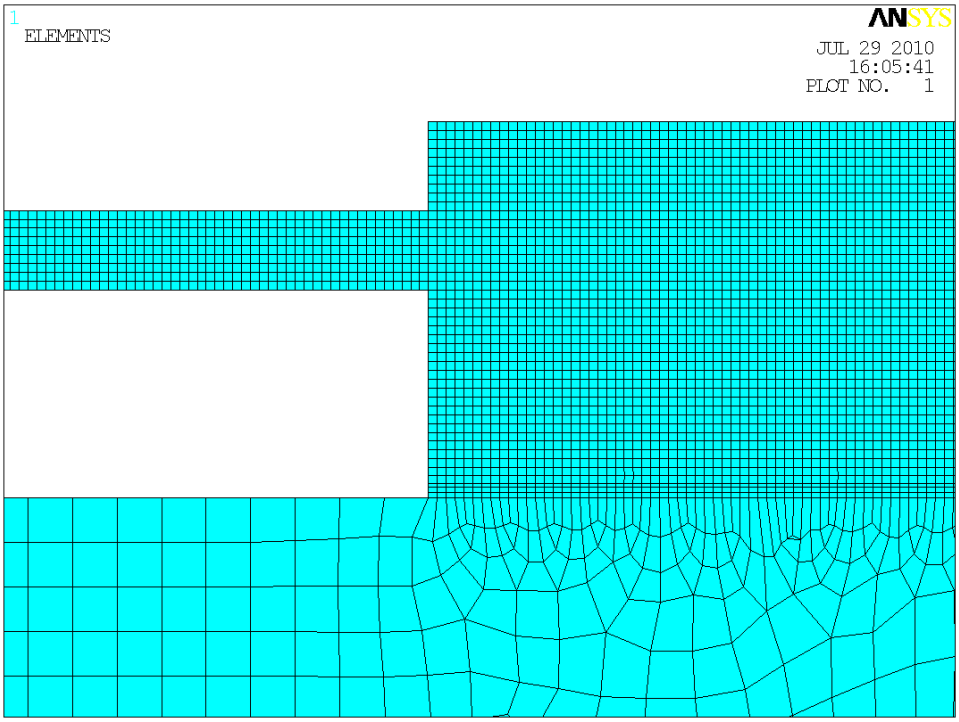


Fig. 6: The mesh model of the bridge structure

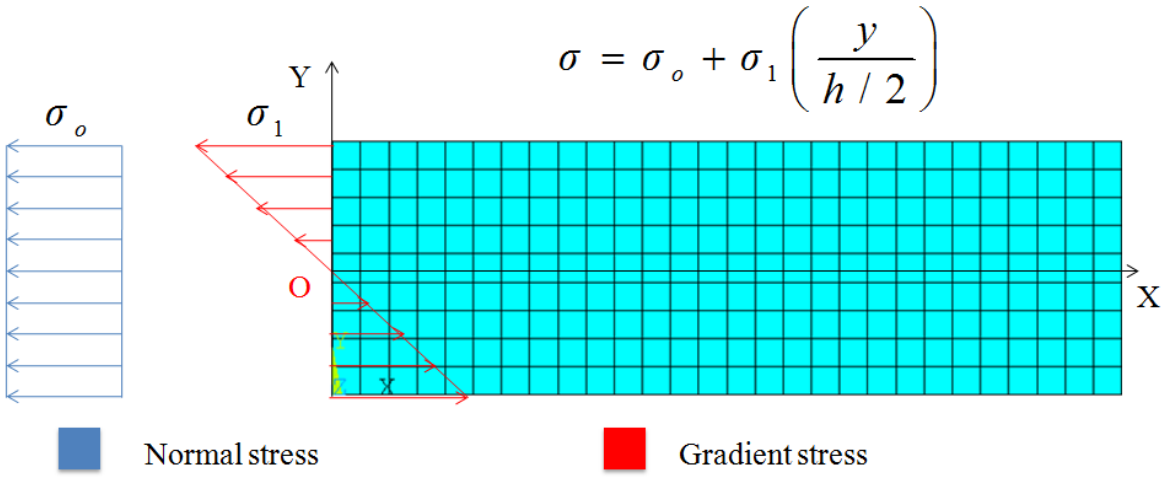


Fig. 7: The schematic diagram of the residual stress inside the thin film

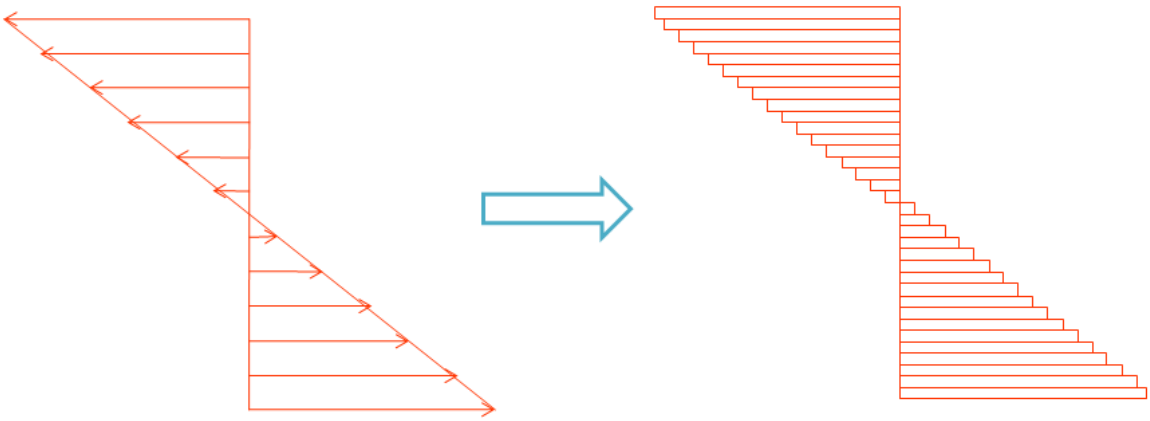


Fig. 8: The approximated method of gradient stress

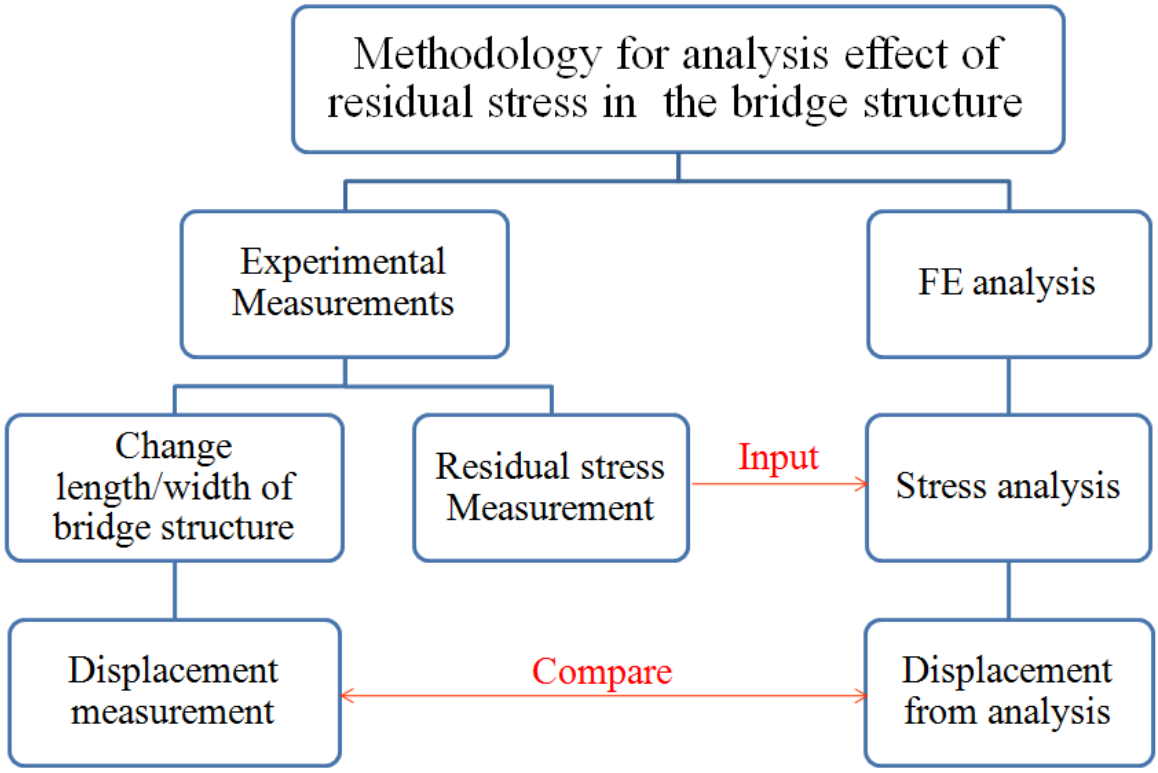


Fig. 9: Methodology of the residual stress detective method of this study

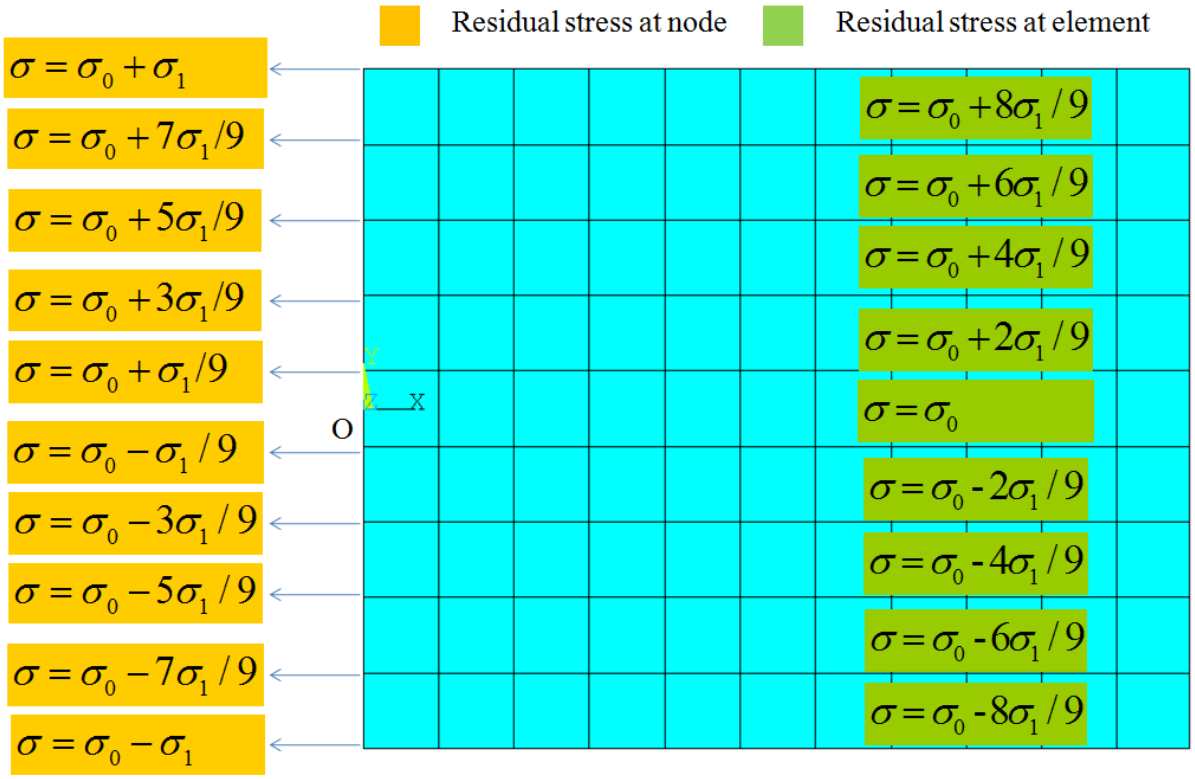


Fig. 10: The detailed stress combination in the M2 layer film

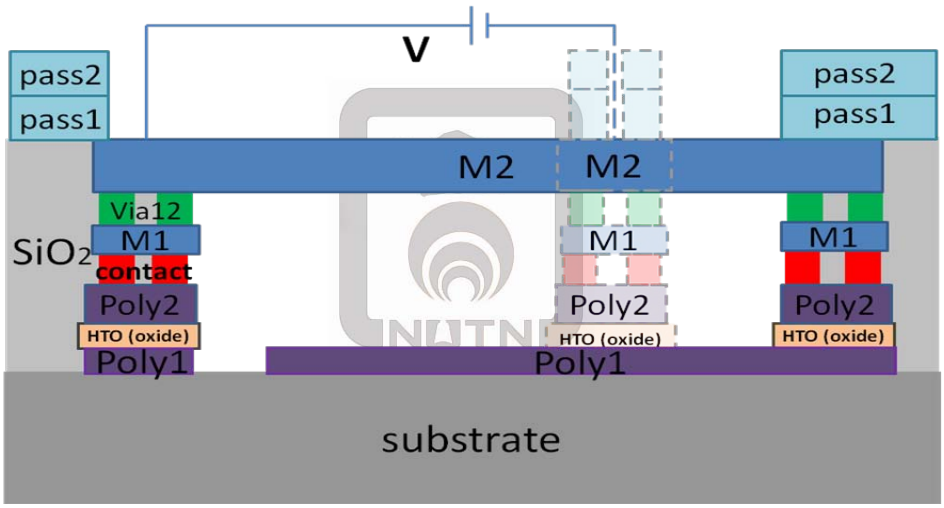
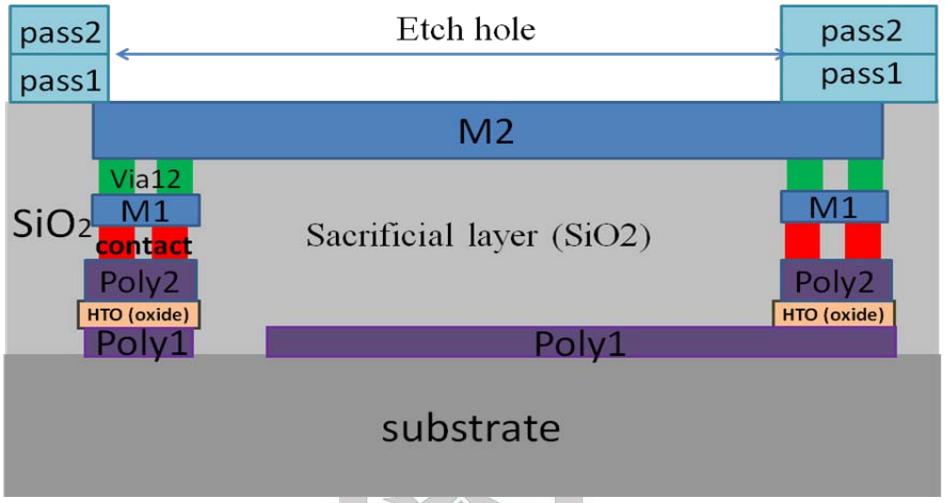


Fig. 11: Schematic of the micro fixed-fixed beam [22]

(a)



(b)

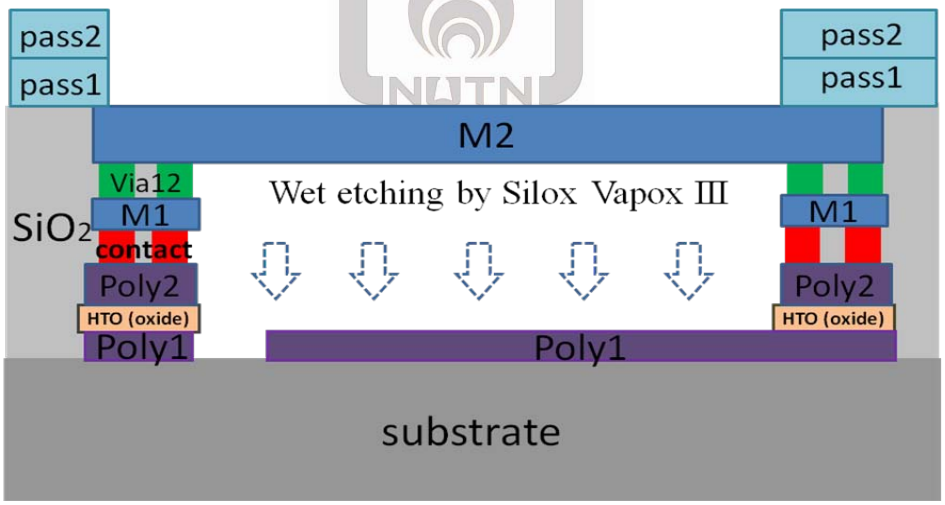


Fig. 12: Schematic cross-section of the micro fixed-fixed beam of the chip, (a) after the CMOS process; (b) after post-processing [22]

Fig. 13: SEM : JEOL JIB-4500 Dual Beam System [24]

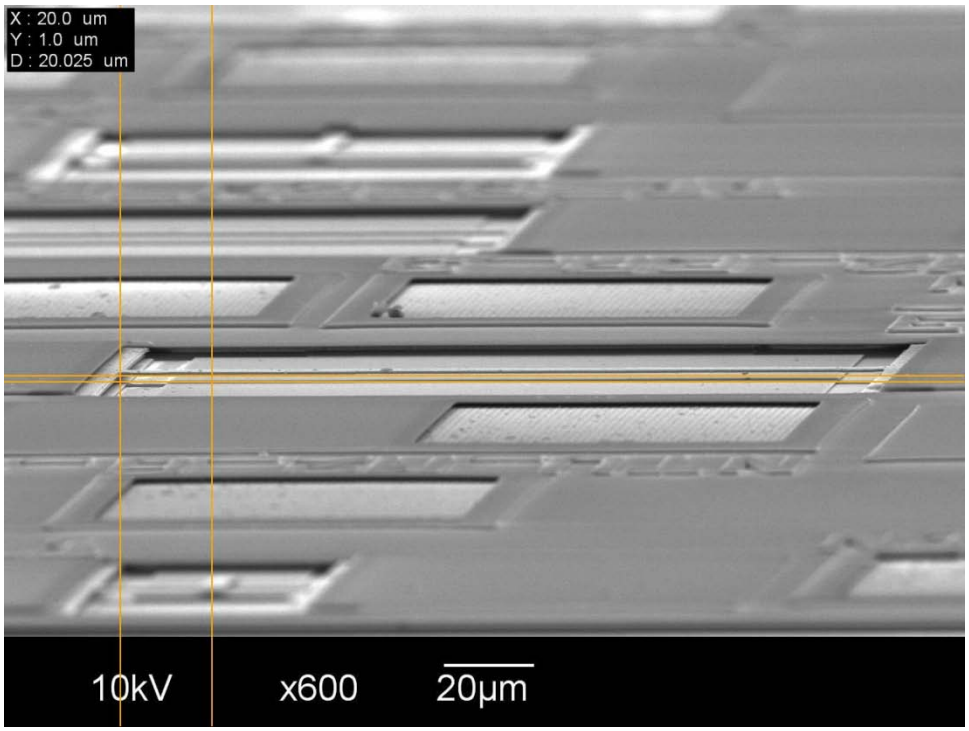
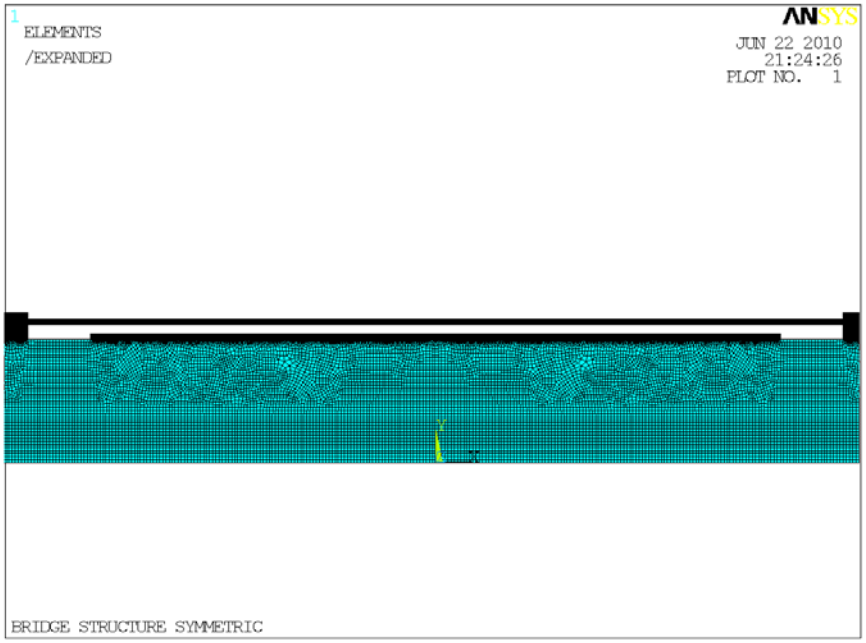
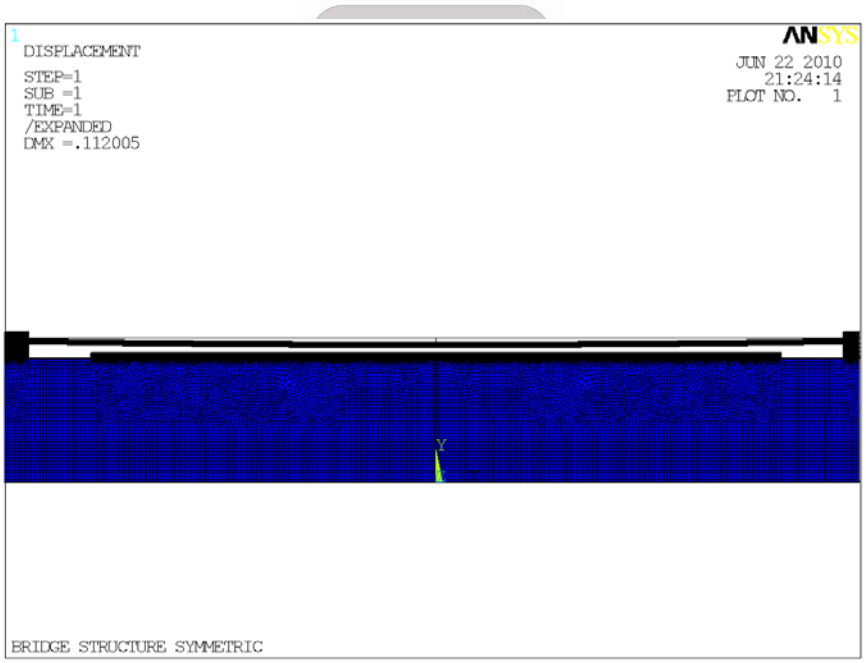


Fig. 14: The measurement of the deformation by using SEM image analysis [22]



a. Before released stress



b. After released stress

Fig. 15: The finite element model of the bridge structure before (a) and after released (b) residual stresses

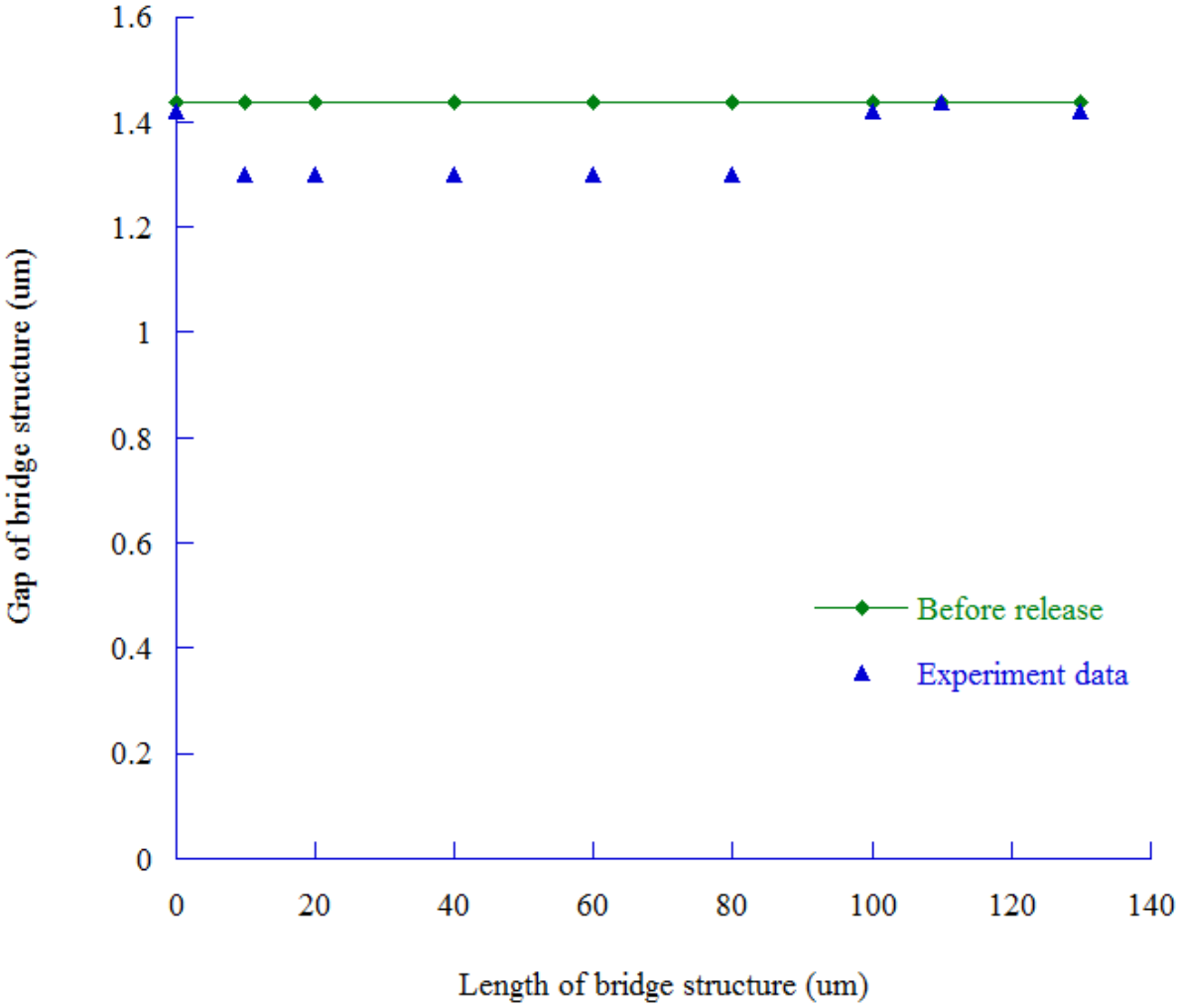


Fig. 16: The deformation of the bridge structure with L = 130μm in experiment

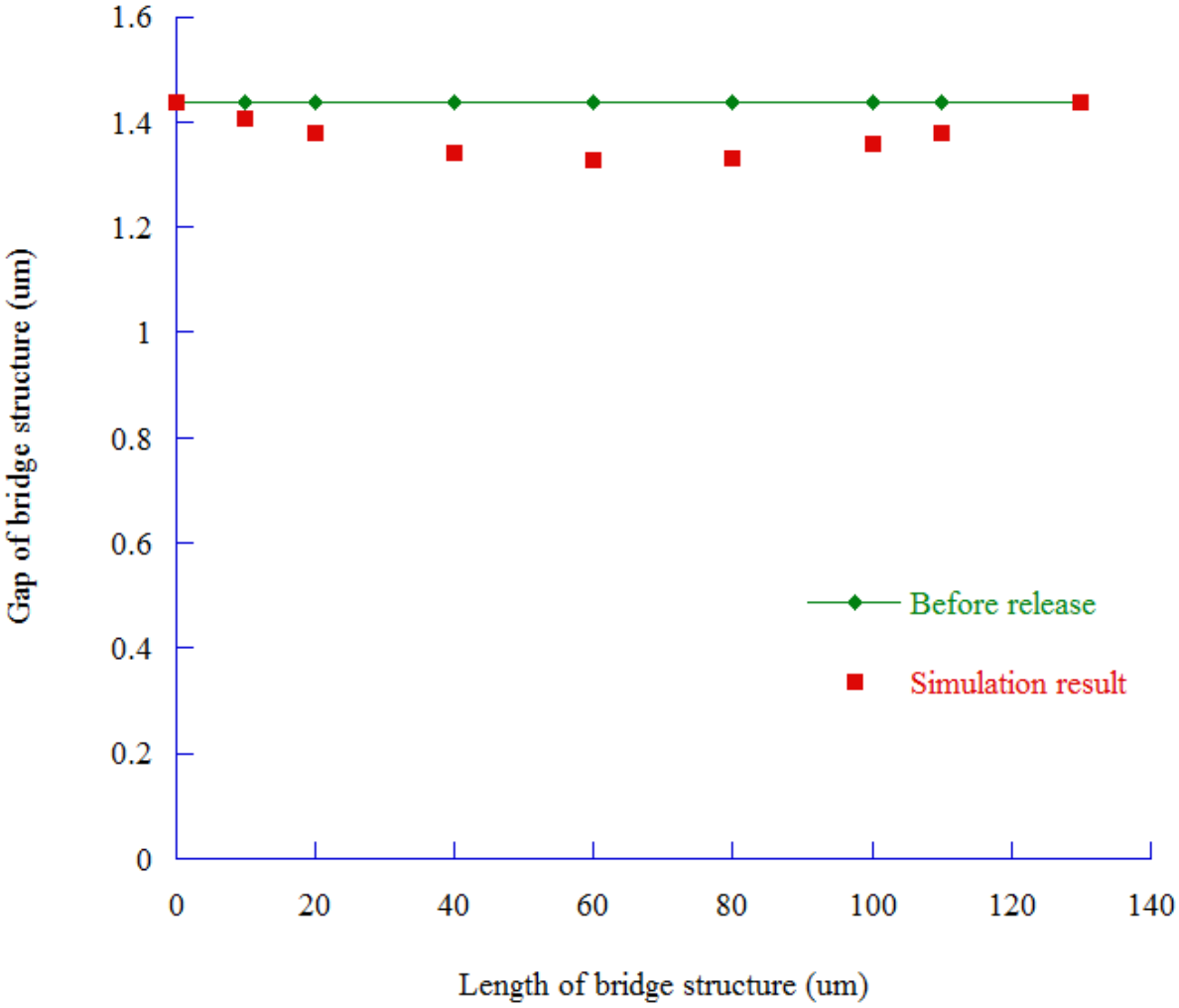


Fig. 17: The deformation of the bridge structure with L = 130μm in simulation

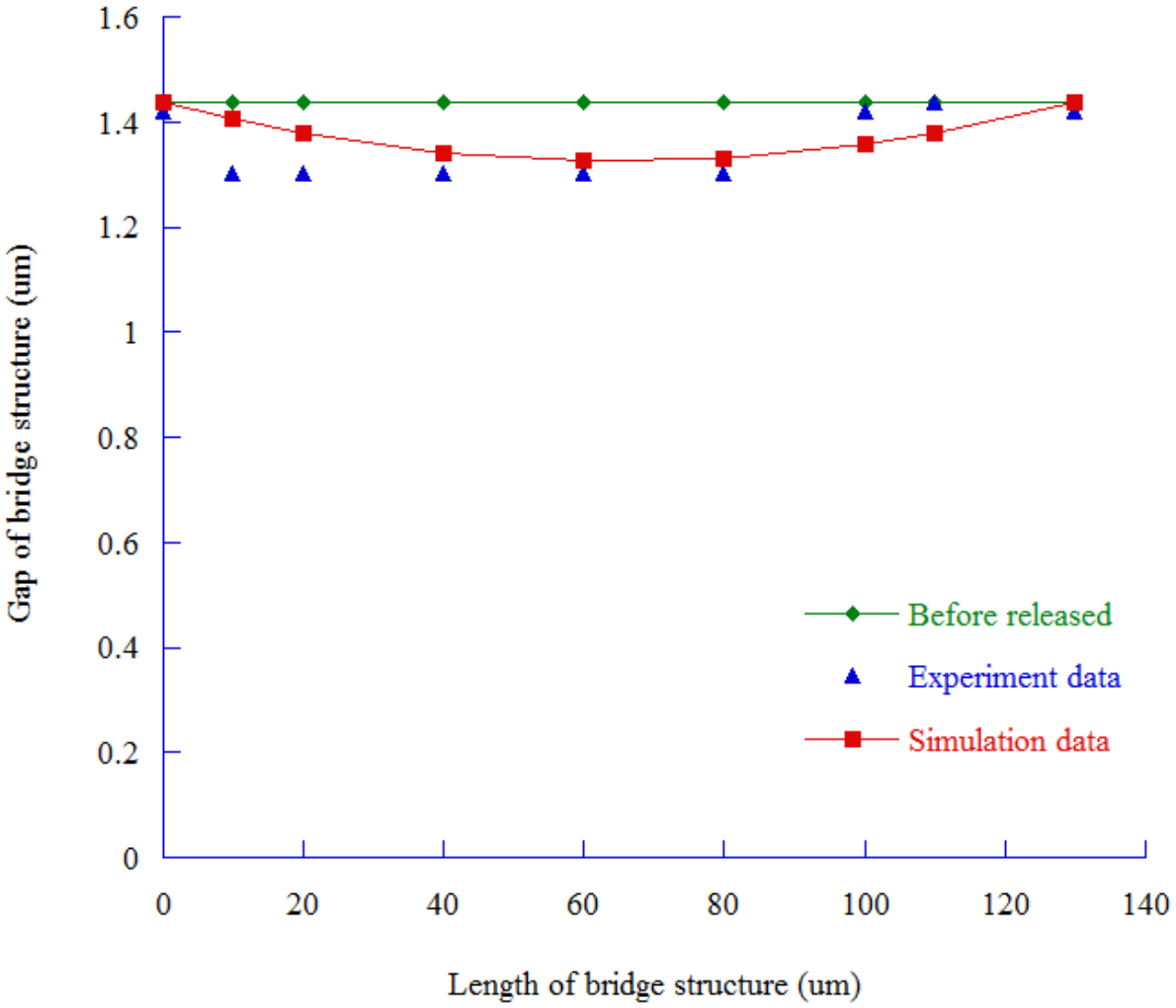


Fig. 18: The comparison between experimental data and simulation result of the 2P2M bridge structure with L = 130µm

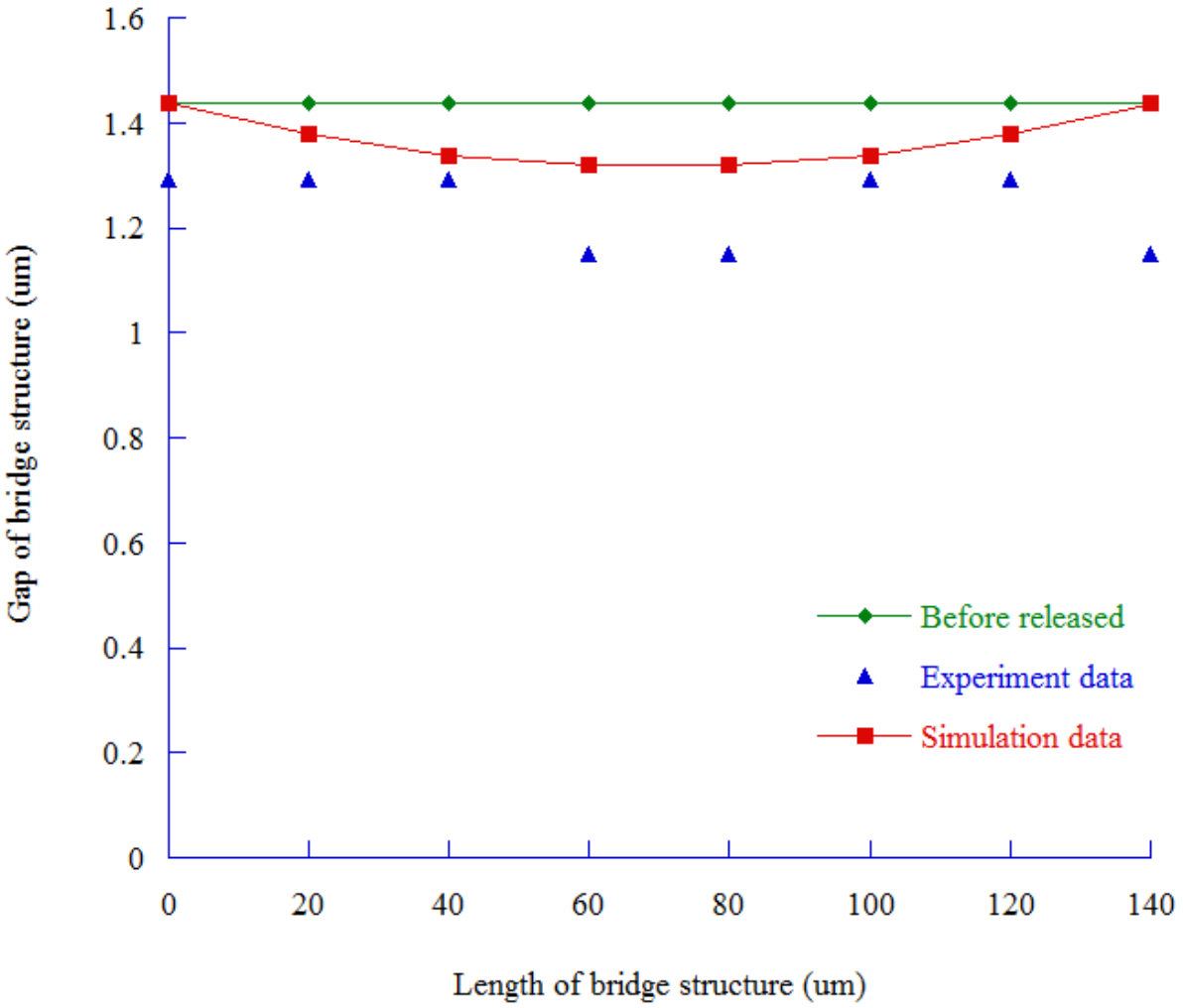


Fig. 19: The comparison between experimental data and simulation result of the 2P2M bridge structure with L = 140µm

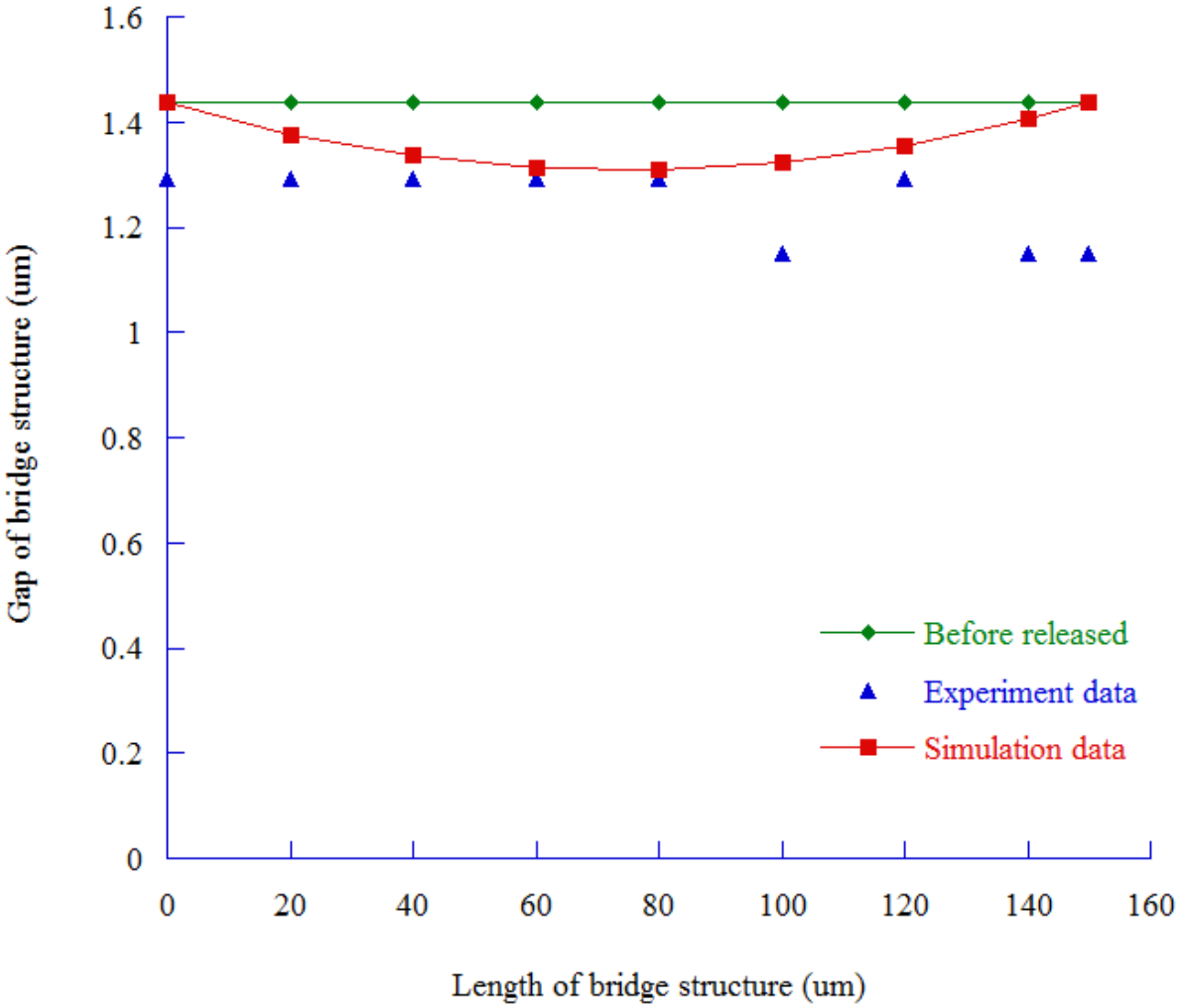


Fig. 20: The comparison between experimental data and simulation result of the 2P2M bridge structure with L = 150µm

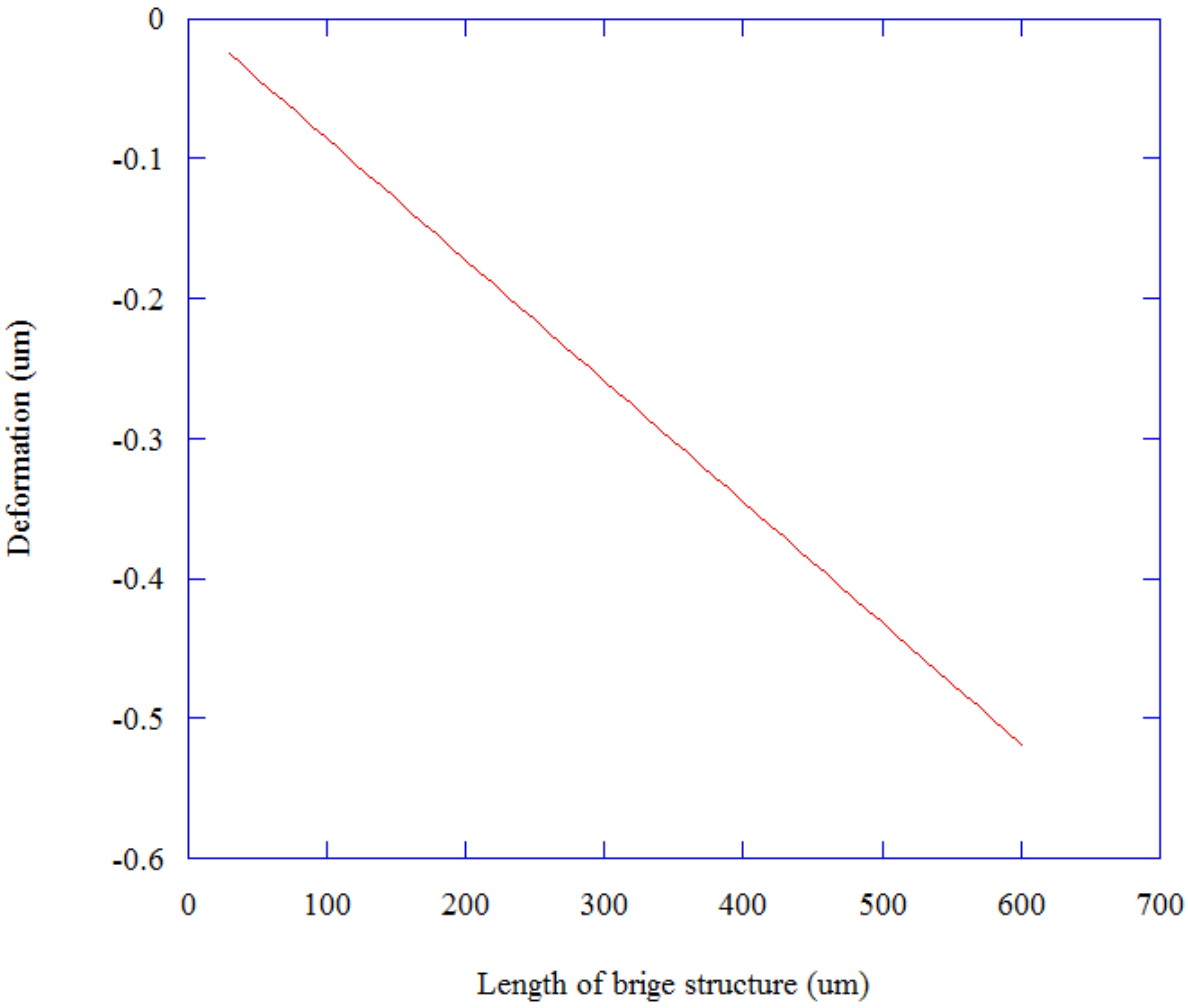


Fig. 21: Relationship between deformation and length of the 2P2M bridge structure in simulation

3. A METHOD INTEGRATING OPTIMAL ALGORITHM AND FINITE ELEMENT METHOD ON CMOS RESIDUAL STRESS

3-1 Introduction

The progress of silicon integrated circuit (IC) technology has enabled the reliable and cost – effective batch fabrication of highly complex ICs with structures in the micrometer range. In the seventies, it was demonstrated that silicon wafer material can also be used to produce pm – sized mechanical components [26]. The successful combination of electrical devices with mechanical microstructures has led to the rapidly growing field of Micro Electro Mechanical Systems (MEMS). Mechanical components in MEMS are thin film plate and beam structures, fabricated using silicon bulk micromachining or surface micromachining [27 – 28]. The mechanical behavior of these structures is determined by the mechanical properties of the thin films involved, such as Young's modulus and Poisson's ratio…determine the static and dynamic mechanical behavior of the structures [29]. In addition, the thermo - mechanical behavior is influenced by the Coefficients of Thermal Expansion (CTE) of the materials [30]. A cost – efficient approach to the fabrication of MEMS is the application of established IC processes such as Complementary Metal Oxide Semiconductor (CMOS) technology [31 – 32]. Nowadays, MEMS sensors have gained much attention because of their wide range of applications, due to their advantages of low cost, low weight, low power and high quality [33 – 34]. However, the production of low cost MEMS products requires monolithic integration and compatibility with CMOS technology.

CMOS technology is the dominant technology in the global integrated circuit industry. It yields products with low power dissipation and is nearly ideal as a switching device. CMOS technology was first established by J.LILIENFIELD as early as 1925, and then known as MOS field-effect, Later, an improved version, closely similar to present CMOS technology, was introduced by O – HEIL in 1935. Up until 1967, two inventions using CMOS Technology were officially patented for commercial use by WEIMER (1962) and WANTASS (1963). CMOS technology is a technology for constructing integrated circuits. It is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. It is also used for a wide variety of analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication. Over the past 15 years vary rapid progress has taken place in the field of microelectronic. Thus the power of the chip challenges human imagination. The CMOS technology became the leading technology in the circuit industry.

The CMOS fabrication is high technology that base on coating technique that has become an important part of modern industry. The technology, which has proved useful and cost effective, basically involves coating of a component referred to as the substrate with a molten or semi-molten material possessing good physical properties. During the CMOS fabrication process, residual stress is generated due to thermal mismatch develops in thin film deposited process (layer by layer deposited on silicon substrate). Residual stress introduced from curing was determined by thermal contraction as a result of cooling from the curing temperature to room temperature. The residual stress is not only created when CMOS process finish but also appears in each step on fabrication process and it has great influence on the full process of design, fabrication and package of the devices. Residual stress may damage a microelectronic during CMOS fabrication and/or reduce its service life. The large value can cause cracks in

the film or delamination of the film from the substrate. Various factors contribute to residual stress generation and these can be material or process dependent. Residual stress is also generated through the rapid solidification and eventual cooling of molten droplets impinging and spreading on a substrate or previously deposited layer.

Nowadays, many modern experiment methods are determined residual stress, common is curvature method, diffraction (X-ray diffraction, neutron diffraction, electron diffraction), etc. Parallel experimental method, Finite Element Analysis (FEA) method can determine the distribution and value of residual stress correctly with low cost, reduce time and get big benefit. By using “Birth and Death” method in ANSYS software (ANSYS Inc., SOUTHPOINTE, PA, USA), it not only determines the value and distribution of residual stress but also illustrates characteristic of residual stress, various factors which contribute to residual stress generation in CMOS fabrication process very clearly and correctly. With this method the free and reactionless (death) movement of a solid structure on deformed geometries and the activation of this solid structure at later simulation steps (birth) is possible. For demonstrating the benefit, this method was applied to simulate the thermal induced bending of multilayer coatings. The “birth and death” method is more accurate than standard bulk approaches because it is possible to calculate the influence of layer deposition on deformed substrates. In the simulation, the geometry was updated layer by layer, the temperature and displacement is analyzed in the same time. An optimal method is also used for reducing residual stress in the CMOS fabrication. The optimum design of this study uses the finite element method combined with the simplified conjugated gradient method (SCGM) to find the minimization of Von Mises stress in CMOS fabrication at room temperature.

3-2 CMOS fabrication literature review

Complementary Metal Oxide Semiconductor (CMOS) process includes many thin film deposited on silicon substrate [35]. Thin films on semiconductor substrates are of special interest to the microelectronic industries. Characterizing mechanical properties of thin films has become a very active area of research. The U.S. Materials Research Society has organized seven symposiums on “Thin Films: Stresses and Mechanical Properties” since 1988 [36].The CMOS fabrication bases on coating technique that is commonly used in a wide range of applications and industrial products. Multilayer coatings can be used as mechanically deformed plates in surface micro machined systems [37] and are commonly used in micro system technology. During CMOS fabrication process, residual stress due to thermal mismatch develops in thin film deposited process. It can affect the mechanical properties and long-term electrical performance of sensors [38]. Residual stress is not constant, and usually depends on experimental and environmental factors such as fabrication, temperature, pressure and time [39 – 40] and may damage a microelectronic device during its fabrication and/or reduce its service life. The large value can cause cracks in the film or delamination of the film from the substrate. Moreover, residual stresses in thin films deposited on substrates are an important on the reliability of film/substrate systems [41 – 43].

The residual stress in the deposition consists in the summation of the intrinsic stress and the thermal stress [44 – 45], where the former is induced during the film – growth process and the later is caused by the mismatch of Coefficient of Thermal Expansion (CTE) between the films and the substrate. In general, thermal effects provide considerable contributions to film stress. Therefore, film stress and CTE are important mechanical behavior in the areas of Micro – Electronics and Micro – Electro – Mechanical Systems (MEMS) [46 – 47]. The CTE describes the relative elongation per temperature change of a stress – free body [48] and the

difference among CTE of the multilayer can create complicated residual stresses in the finished CMOS – MEMS devices. There are several problems that arose from the thermal expansion effect, for instance, the mismatch of thermal expansion between the thin films and the substrate may lead to residual stresses in the thin films [49]. Thus, the electronic devices as well as the micro – machined structures will be damaged or deformed by this effect. In order to design micro – machined components as well as microelectronics devices properly, it is necessary to characterize the CTE for thin film materials.

Residual stress in the CMOS fabrication is a stress under no external loading and is the sum of growth stress and thermal stress. The various physical parameters of both the deposited layers and the substrate on which thermal stress depends can be listed as coefficient of thermal expansion (CTE), Young's modulus, Poisson's ratio, thickness, thermal conductivity, temperature histories during deposition and cooling and stress relaxation mechanisms. In general, thermal stresses develop at the interface between deposited layers and substrate [50]. Generally, analytical equations have been developed to describe the biaxial thermal stress states in coating substrate system for linear–elastic or simple elastic–plastic materials [51-52].

Recently, for a more general 2D or 3D problem numerical methods such as finite element analysis (FEA) has been accepted as an attractive tool to simulate residual stress in coating technology. To consider nonlinear deformations and respect the layer deposition on deformed substrates finite element analysis (FEA) has to be utilized. Stressless layers deposited on already deformed multilayer have to be simulated with the so called “birth and death” method. Birth and death method is special method in ANSYS [53]. It can be used to simulate in manufacturing process [54], welding process [55 – 56] and especially in coating [57]. This method is predefined in other commercial FEA – programs and causes the free and

reactionless (death) entrainment of layers deposited later on. The free and reactionless movement of layer – elements can be switched into a mechanically active status (birth) at the simulation step where the layer should be deposited. The drawback of the previous papers is that the simulation of the fabrication process is just steady – state. It means that the temperature load at each step is kept constant and there isn't heat transfer among the thin film layers and substrate. It can't also reflect the effect of the cooling speed in the fabrication process.

Nowadays, having many modern experimental methods to estimation residual stress, common is: X-ray and neutron diffraction, strain/curvature measurements, layer removal, Raman spectroscopy [58 – 59] with purpose estimate residual stress. Parallel experimental method, FEA method can determine the distribution and value of residual stress correctly with low cost, reducing time and getting big benefit.

In this thesis, an optimal method is used for reducing residual stress in CMOS fabrication. The optimization is used to search the extreme value of the objective function. The optimal methods currently used can be broadly divided into two categories: one is the gradient based techniques, such as the gradient search method (GSM) [60] and the conjugate gradient method (CGM) [61, 62]. These methods can generate the local or global solution by the different initial values, and these methods have the advantage of the faster convergence. The other is the simulated evolutionary optimization, such as the genetic algorithms (GA) [63] and the simulated annealing (SA) [64, 65], which can search the global solution, but needs a lot of iterations to convergent. This research is to demonstrate how the application of numerical optimal simulation techniques can be used to search for an effective optimization of CMOS fabrication. Therefore, the optimal design obtain the minimum residual stress is achieved in the present study.

The numerical design approach is developed by combining a direct problem solver, ANSYS code, with an optimization method (the simplified conjugate gradient method, SCGM). A finite element analysis model ANSYS is used as the subroutine to solve the stress-strain profile associated with the variation of the parameter of the CMOS fabrication during the iterative optimal process. The SCGM method, proposed by Cheng and Chang [66], is capable of obtaining the minimized objective functions easily, and calculating fast than traditional conjugated gradient method. In the SCGM method, the sensitivity of the objective function resulted from the designed variables is evaluated first, and then by giving an appropriate fixed value for the step size, the optimal design can then be carried out without overwhelming mathematical derivation. This study is aimed at the optimization residual stress of the CMOS fabrication.

According the above citing references, we can notice that this study develops birth and death method to predict the residual stress in the CMOS fabrication process. As the same time, the transient analysis is proposed to reflect the heat transfer process also the cooling speed effect in the CMOS fabrication. In the addition, the issue of the CMOS fabrication process optimal design is very important. This study also proposes the optimal design fabrication process by using SCGM to reduce the residual stress in the CMOS fabrication process.

3-3 Numerical analysis and modeling

3-3-1 Birth and death method in coating technique using ANSYS

In MEMS field, two principal micro fabrication processes for microstructures are: (1) Type A: Adding materials to the substrate by deposition processes, (2) Type B: Removing material of the substrate by etching processes. By using the DEATH elements, parts of the structure are created by type B as the death elements in the FE mesh for the finished structure geometry, following Fig. 22a. Similar, parts of the structure are created by type A as the BIRTH elements that are described in Fig. 22b. Death and birth elements can be combined to illustrate overall structure (Fig. 22c). Both “Death” and “Birth” elements are originally included in the FE mesh of the “finished” overall structure of the micro component, with the following distinguished material properties. For “death” elements: Initial properties are the same as the substrate material, e.g. switched to low Young’s modulus, E = 0+ and density ρ, but high yield strength, σ_y at the end of the predicted time for etching. And for “birth” elements: The assigned material properties, e.g. the Young’s modulus, density and yield strength are switched in the reverse order as in the case of “death” elements at the end of the deposition process.

To achieve the "element death" effect, the ANSYS program does not actually *remove* "killed" elements. Instead, it *deactivates* them by multiplying their stiffness (or conductivity, or other analogous quantity) by a severe reduction factor. Element loads associated with deactivated elements are zeroed out of the load vector. However, they still appear in element-load lists. Similarly, mass, damping, specific heat, and other such effects are set to zero for deactivated elements. The mass and energy of deactivated elements are not included in the summations over the model. An element's strain is also set to zero as soon as that element is

killed. In like manner, when elements are "born," they are not actually *added* to the model, they are simply *reactivated*. You must create all elements, including those to be born in later stages of your analysis. To "add" an element, you first deactivate it, and then reactivate it at the proper load step. When an element is reactivated, its stiffness, mass, element loads, etc. return to their full original values. Elements are reactivated having no record of strain history (or heat storage, etc.). Thermal strains are computed for newly-activated elements based on the current load step temperature and the reference temperature.

3-3-2 Model description

Fig. 23 shows the illustration and Scanning Electron Microscope (SEM) picture of CMOS-MEMS Microphone, the corresponding simplified coess-section is presented in Fig. 24. Layer deposition in micro - system technology occurs normally on thicker (typically: 400 µm to 675 µm) substrates. Due to the geometric aspect ratio of the deposited layer thickness to the substrate thickness this value was chosen 60µm to get extreme fine meshing and computing power respectively. Furthermore the thin substrate enhances the effect of the layer deposition on bended substrates.

To evaluate the residual stress distribution within CMOS fabrication, a finite element model was developed using ANSYS 11. PLANE13 is a 2D coupled – field solid element and it is defined by four nodes with up to four degrees of freedom per node was selected for the analyses. To develop FE model, the PLANE13 element has been used as an axisymmetric element having X displacement (UX), Y displacement (UY) and temperature (TEMP) as degrees of freedom at each node. The detail material characteristics of each layer in CMOS process are given in tables 7 – 8 [35]. Aluminum is non-linear material which has Young's modulus depend on temperature, is used in the FE calculation by assuming a "bilinear hardening behavior". The Young's Modulus Aluminum was described in Fig. 25. In the other

hand, it is important to use a consistent system of units for all the data. For MEMS, components may be only a few microns in size, so this paper uses the conversion factors from standard MKS to μMKSV.

The FE mesh was constructed to include the substrate and the final thickness of coating. After meshing the domain, the elements in the coating were then deactivated causing elimination of the elements. For every incoming layer, the dead elements representing that splat were activated a layer at a time. The finite elements mesh of the model for the above seven layer coating. The quadrilateral mesh for the model consists of 750 columns of elements in the horizon direction with 120 rows of elements through the substrate thickness and 3 rows of elements for each layer. The detail demonstrates in Fig. 26.

3-3-3 Boundary condition

A symmetric model was employed to reduce data processing time; it's described in Fig. 26. Only half of CMOS device is analyzed due to the symmetry boundary condition: along the line of the symmetry, displacement in x direction is confined ($U_x = 0$); the node is at the bottom most nodes, no displacements occur in all direction ($U_x = 0$, $U_y = 0$) to prevent a rigid body motion. Fig. 27 shows the deposition parameters about the simplified CMOS fabrication. Fig. 28 illustrates thermal condition in detail. This process is the coupled thermal – structural process, it includes structure constraint and thermal condition.

3-3-4 Residual stress in CMOS fabrication

Residual stress includes the quenching stress and thermal stress. The quenching stress is due to the rapid contraction of the deposited layer cooled from operating temperature to substrate temperature. The magnitude of quenching stress can be estimated [67]:

$$\sigma_q = \alpha_c (T_m - T_s) E_c \tag{3.1}$$

where: α_c, E_c, T_m, T_s are coefficient of thermal expansion (CTE), elastic modulus, melting point of the deposited material and substrate temperature, respectively.

The thermal stress induces by the mismatch in CTE of the substrate and deposited materials. Thermal stress at the interface can be estimated by [68]:

$$\sigma_{tc} \approx E_c \Delta\alpha \Delta T \frac{1+\nu}{1-\nu^2} \tag{3.2}$$

where: $\Delta\alpha$, ΔT and ν are the CTE mismatch between the substrate and deposition layers, the temperature drop in the cooling and the Poisson's ratio, respectively.

The overall magnitude of residual stress in CMOS fabrication is the summation of quenching stress and thermal stress

$$\sigma_{\text{residual}} = \sigma_q + \sigma_{tc} \tag{3.3}$$

3-3-5 Validated model

A validated study is designed to explore the correctness, excellence of the proposed method in this study. First, we build a model and compare with the previous study [57] to validate the correctness of method. The validated model consists of two layer deposited on silicon substrate. The comparison between the previous study and our model provides the verification for the “birth and death” method simulation. In the previous study, the author used COMSOL package to simulate the coating process in MEMS. The fabrication includes 2 layers (SiO_2 and Aluminum) deposited on the silicon substrate with different temperature deposition. Fig. 29 shows the model and constraint with substrate thickness is 20µm, SiO_2 and Al layer thickness is 1µm. Fig. 30 shows the fabrication process of this model. At the first step, the silicon plate is heated up to 900°C as the thermal grow of 1 µm silicon oxide (SiO2) occurs. Afterwards the two layers are cooled to room temperature. Since the second process, the temperature decreases to 400°C, the deposition of 1 µm aluminum (Al, third step) occurs

on the curved surface. At the final process step the three layered stack is cooled down to room temperature.

In previous paper, the free and reactionless movement of death layer elements is done by applying a very low YOUNG's modulus in COMSOL package and the activation of the elements is realized by switching the YOUNG's modulus back to the physical material value. At the period 2, the temperature decrease from 900^{o}C to 400^{o}C to make bending down the stack. The y displacement distribution is described in Figs. 31(a-b). Fig. 32 shows the y - displacement depending on the lateral displaced x - position after the deposition of the thermal silicon oxide on silicon substrate. The resulting surface deformations are consistent for the ANSYS and COMSOL package models. Through this figure, the maximum deformation by using ANSYS and COMSOL package is -0.321µm and -0.318µm, respectively. The comparison with previous paper at 11 specific positions is proposed in table 9 in detail. It finds that the simulation result in ANSYS package agree well with previous paper. The deviation is also calculated in the table 9. The average deviation is 0.66%.

At the period 4, the stack is cooled down to the room temperature (25^{o}C) after finishing deposition of aluminum. It is notice that the simulation must respect the aluminum deposition on the deformed substrate. Figs. 33(a-b) show the y displacement distribution in COMSOL and ANSYS at the room temperature, respectively. In addition, Fig. 34 illustrates the y - displacement depending on the lateral displaced x - position after deposition of the aluminum layer consisting for the ANSYS and COMSOL package models. Through this figure, the maximum deformation by using ANSYS and COMSOL package is 0.806µm and 0.8µm, respectively. The comparison with previous paper at 11 specific positions is proposed in table 10 in detail. It finds that the simulation result in ANSYS package agree well with previous paper. The average deviation is 0.66%. It is shown in the table 10.

According to this comparison, the above investigation makes a conclusion that the “birth and death” method is to be clear about the proof that credibility of simulation is sufficient for this research. By using the birth and death element, it can respect the aluminum deposition on the deformed substrate in the fabrication. If it is impossible to calculate the influence of the layer deposition on deformed substrates, the simulation of the fabrication process will be wrong. Fig. 35 shows the curvature’s comparison between method with and without birth and death element at room temperature. Through this figure, the resulting surface deformation is so different and the maximum deformation by using method with and without birth and death element is 0.806μm and 0.479μm, respectively. The comparison between the method with and without birth and death element at 11 specific positions is illustrated in table 11 in detail. The average deviation is 55.92%.

3-3-6 Simulation methodology

When analyzing, it is more flexible to create the model by editing program files (APDL – ANSYS Parametric Design Language) rather than by working through the Graphic User Interface (GUI). It is much easier to change the model geometry and physical parameters in the program files. ANSYS Parametric Design Language is a scripting language that you can use to automate common tasks or even build your model in terms of parameters (variables). APDL also encompasses a wide range of other features such as repeating a command, macros, if-then-else branching, do-loops, and scalar, vector and matrix operations. While APDL is the foundation for sophisticated features such as design optimization and adaptive meshing, it also offers many conveniences that you can use in your day-to-day analyses. In this guide we'll introduce you to the basic features- parameters; macros; branching, looping, repeating and array parameters.

Residual stresses resulting from a transient analysis consider both thermal and quenching stresses. Heat transfers were considered to be time-dependent. Convection to the surrounding environment was used as thermal boundary condition. The heat flux from the heat source was neglected, considering that each layer was exposed to high temperature for a short duration. In Fig. 36, flowchart illustrates the method with using "birth and death" element to simulate CMOS fabrication process. When new layer is deposited, these elements were assumed to be in solid phase at melting temperature or semi – melting temperature, implying that contraction of the elements when they were in liquid phase did not generate significant stresses. The melting points (or semi – melting points) of deposited layers were assumed to be the stress-free reference temperature. The element type selected to simulate the growth of deposited layers was PLANE13 that is suitable for combined thermal/structural analysis and offers the capability of birth/death element function. In each step of CMOS fabrication as a thin layer of material was deposited onto the surface, a layer of elements with the corresponding thickness was activated through the 'birth' function. For n deposited layers, n-1 period which deal with the same geometry, mesh and mechanical clamping have to be set up. Only layers have already deposited or currently deposited are set "birth element". The layers above refer the death option. For the currently deposited layer, set it is birth element from the death layer at the previous step and every layer in each period keeps its reference temperature.

Table 12 shows the detail step by step simulation of CMOS fabrication. First, heating the silicon substrate to oxidation temperature and thermal grow of SiO_2. At the 1^{st} period mode, the thermal contraction of silicon oxide on silicon is included for the temperature decrease from Temperature reference = 980^oC to Temperature = 620^oC (620^oC is deposited temperature of 2^{nd} layer – Polysilicon). The other layer set "death element". The 2^{nd} period mode, Polysilicon is set "birth" and the other layer which isn't deposited still set "death". The

3rd period mode is similar the 2 period mode previous… After all layers had been deposited, the CMOS was cooled to room temperature (25^0C).

3-3-7 Optimization method

For the purpose of the optimum design, the objective function J of this study is the minimum Von Mises stress in the CMOS fabrication. The Von Mises stress (as known as equivalent stress σ_{eqv}) is given by:

$$J = \sigma_{eqv} = \sqrt{\frac{(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_3 - \sigma_1)^2}{2}} \tag{3.4}$$

where σ_1, σ_2 and σ_3 are principle stresses. Beside, IA is the iteration number in the optimal design process.

In addition, we assume $\{a_i, i=1,2,\ldots,l\}$ the set of the undetermined coefficients. The variables a_i are treated as the optimal variables which are to be designed in this study to minimize the objective function. Different combinations of these coefficients represent the variation of the fabrication process. In other words, in the optimization process, the undetermined coefficients are updated iteratively toward the minimization of the object function.

In this manner, as the objective function is approaching its minimum value in the optimization process, with the definition of J, the equivalent stress gradually reaches a minimum value. This implies that the phenomena of the residual stress will be decreased.

The minimization of the objective function is accomplished by using the SCGM method. The method evaluates the gradient functions of the objective function and sets up a new conjugate direction for the updated undetermined coefficients with the help of a direct numerical sensitivity analysis.

We perform the direct numerical sensitivity analysis to determine the gradient functions $\left\{\left(\partial J/\partial a_i\right)^n,\ i=1,2,...,l\right\}$ in the n_{th} step. First, give a perturbation $\left(\Delta a_i\right)$ to each of the undetermined coefficients, and then find the change of the objective function $\left(\Delta J\right)$ caused by Δa_i. The gradient function with respect to each of the undetermined coefficients can be calculated by the direct numerical differentiation as

$$\frac{\partial J}{\partial a_i}=\frac{\Delta J}{\Delta a_i} \tag{3.5}$$

Then, we can calculate the conjugate gradient coefficients, γ_i^n, and the search directions, π_i^{n+1}, for each of the undetermined coefficients with

$$\gamma_i^n=\left[\frac{\left(\dfrac{\partial J}{\partial a_i}\right)^n}{\left(\dfrac{\partial J}{\partial a_i}\right)^{n-1}}\right]^2,\quad i=1,2,\ldots,l \tag{3.6}$$

$$\pi_i^{n+1}=\left(\frac{\partial J}{\partial a_i}\right)^n+\gamma_i^n\pi_i^n,\quad i=1,2,\ldots,l \tag{3.7}$$

The step sizes $\left\{\tau_i,\ i=1,2,...,l\right\}$ will be assigned for all the undetermined coefficients and leave it unchanged during the iteration. In this study, the fixed value is determined by a trial and error process, and the value is set to be 1.0×10^{-6} typically. The difficulty lies with the fact that how to decide the suitable value of the step size. The undetermined coefficients will be updated.

$$a_i^{n+1}=a_i^n-\tau_i\pi_i^{n+1},\quad i=1,2,...,l \tag{3.8}$$

The procedure for applying the SCGM method is described briefly in the following:

(1) Make an initial guess for the shape profile by giving initial values to the set of undetermined coefficients. With initialization accomplished, the run itself can begin.

(2) Use the direct problem solver to predict the residual stress and stress distribution of the CMOS deposited layer by Eq. (3.4).

(3) When the objective function reaches a minimum, that is to say, the relative criteria is satisfied, the solution process is terminated. Otherwise, proceed to step (4).

(4) Through the Eq. (3.5), to determine the gradient functions.

(5) Through the Eqs. (3.6) and (3.7), to calculate the conjugate gradient coefficients, γ_i^n, and the search directions, π_i^{n+1}, for each of the undetermined coefficients.

(6) Assign a fixed value to the step sizes for all the undetermined coefficients and leave it unchanged during the iteration.

(7) According the Eq. (3.8), to update the undetermined coefficients and re-new the fabrication condition, and go back to step (2).

It is important to mention that the emphasis of present study is put on the optimization of the CMOS fabrication. The flow chart of the optimization process is plotted in Fig. 37. The self-developed optimizer and the commercial ANSYS code are connected through a script program APDL provided by ANSYS. The changes of the undetermined coefficients were suggested by the optimizer transfers to the direct problem solver for building the updated fabrication condition. Next, the direct problem solver is executed based on the updated information to yield the numerical predictions of the stress fields and the objective function as well, which are further transferred back to the optimizer for calculating the consecutive searching directions.

3-4 Result and discussion

3-4-1 CMOS fabrication

In present study, the aim is to predict the residual stresses in the CMOS fabrication process. The coupled heat transfer and elastic – plastic finite element stress analyses were combined to simulate the generation of the residual stresses during CMOS fabrication process. During the fabrication process, each layer is with the corresponding deposition temperature. After depositing the top layer (SiN), all layers will be cooled by natural cooling (convective to the air). The coefficient of thermal expansion (CTE) mismatch between the silicon substrate and the deposition materials dominates the stress variation during the process steps. Fig. 38 shows us the residual stress Sx variation during the process steps in different thin films of the CMOS-MEMS microphone.

From step 1 (the substrate is heated to 980^{o}C) to step 2 (the first layer FOX start depositing), the residual stress is 0. After finishing deposition of 1st layer, the temperature decrease to 620^{o}C for preparing deposited 2nd layer at step 3. In here, the residual stress is generated in the 1st layer (-54.1MPa). And then the 2nd layer starts depositing at step 4, the residual stress in 1st layer don't change value. After finishing deposition of 2nd layer, the temperature increase to 850^{o}C for preparing deposited 3rd layer at step 5. And now, the residual stress is generated in 2nd layer (-15.3MPa) and the residual stress in 1st layer change to -19.7MPa. In the step 6, the 3rd layer starts depositing and the residual stress in 1st layer, 2nd layer don't change value. After finishing deposition 3rd layer, the temperature decrease to 400^{o}C for preparing deposited 4th layer at the step 7. The residual stress in 1st layer, 2nd layer and 3rd layer is -85.7MPa, 35.1MPa and -51.6MPa, respectively. In step 8, the 4th layer starts depositing and the residual stress in previous layer keeps value. In step 9, the temperature

increase to 500^{o}C and the residual stress is generated in 4th layer, the stress value in 1st - 4th layer is -71.2MPa, 26.4MPa, -40.4MPa and 6.8MPa, respectively. The 5th layer starts depositing in step 10. The residual stress keeps constant. In step 11, the temperature decrease to 400^{o}C. The residual stress is generated in the 5th layer. Similarly, the residual stress in 1st – 7th layer at room temperature is -146.7MPa, -43.5MPa, -115.4MPa, -216.1MPa, 257.5MPa, -200MPa and -101.6MPa, respectively. In each step, the residual stress in each layer is different. It not only depends on the CTE of each layer but also the mismatch of the deposition temperature and the temperature at each step. The largest value of residual stress is at the final step – finishing deposition process and cooling to room temperature (25^{o}C). That's reasonable because the temperature mismatch between deposition temperature and room temperature is largest for every layer.

In the other hand, Fig. 39 illustrates the stress Sx (stress follow X direction) distribution in different layers at room temperature (25^{o}C). The stress Sx in each layer keeps value constant and only changes strongly at near free edge. It concentrates in the aluminum layer that has the huge CTE. Through X location, Sx stress were observed and reached maximum value near the free edge. Besides, the distribution of the stress Sx through thickness from first layer (FOX) to top layer (SiN) of the CMOS-MEMS microphone device at different X position is proposed in Fig. 40. The shape of the stress Sx distribution is similar through the thickness of all layers and the maximum of residual stress Sx is 257.5MPa at location x = 748μm.

In the addition, CMOS-MEMS Microphone failure mechanisms are mainly controlled by the magnitude and distribution of Sx, Sy (stress follow Y direction), and shear stress Sxy at or near the free edge of the model. Fig. 41 demonstrates the residual stress in CMOS fabrication at room temperature after deposition for Sx, Sy and shear stress Sxy components. Note that the stresses distributions were shown in Figs. 41(a) – (c) are enlarged views of the top – right

corner of the model. It was found that the concentrations of the residual stress components are located at different parts of the model. In this figure, the residual stress Sy concentrates at the free edge. The maximum of the tensile stress and compress stress is 111.1MPa and -123.8MPa, respectively. The concentration of shear stress Sxy is also at the free edge but it concentrates at the intersection. The tensile stress and compress stress is 70.9MPa and 96MPa, respectively. So, the cracks could originate at the free edge due to the high concentration of Sy and shear stresses Sxy.

The above cited discuss the generation of the residual stresses in the normal CMOS fabrication process. In here, base on the aluminum material is non – linear material and the residual stress in that layer is larger than yield stress, an analysis of cooling the CMOS fabrication under room temperature is proposed to reduce the residual stress level. Fig. 42 schematically shows the three cases studied. Case A represents the standard deposition process and the residual stresses present at the end of the cooling cycle are shown in Fig. 41. For case B, the simplified CMOS fabrication is cooled to 15^{o}C after the deposition and subsequently it is returned to room temperature by natural convection. For case C, the CMOS fabrication is cooled to 5^{o}C instead. Figs. 43(a) – (c) shows the residual stress at room temperature for cases B. It is clearly to see that the stress distribution presented in cases B is very similar to those of case A (Fig. 41). And in case C, the situation is the same and is described in Fig. 44(a) – (c). However, it is interesting to find that (cases A → B → C), the values of all stress components decreases. From the case A → B → C, the tensile and compress of residual stress component Sx reduces from (-216.1MPa) → (-211.1MPa) → (-205.9MPa) and 257.5MPa → 246MPa → 234.5MPa, respectively. The other components residual stress are also reduced and illustrated in the table 13.

A qualitative explanation for the stress reduction in as follows Fig. 45 schematically shows the constitutive model for the above three cases. The cooling process causes the mismatch of stress – free temperature and cooling temperature to increase, hence can be referred to as a loading process. Corresponding to case A, point A denotes the stress state in the simplified CMOS fabrication at room temperature and the residual stress will be σ_A. However, if the CMOS fabrication is cooled to B, the stress will first increase following the tangent modulus, but finally upon natural convection to room temperature the residual stress will be σ_B, which is lower than σ_A. An even lower cooling temperature at C will result in further stress reduction to σ_C (case C). Possibly, the simplified CMOS fabrication is cooled to temperature T (case D), the residual stress would be minimum at room temperature.

3-4-2 Optimal residual stress in the CMOS fabrication

The aim of this study is to achieve the minimum Von Mises stress in the CMOS fabrication process through SCGM combined with ANSYS. Through the optimization result, the factors affect to residual stress in CMOS fabrication is shown clearly. According to the above simulation results, the parameter of the fabrication process (e.g. temperature deposition, time cooling, etc) effect to the residual stress in the CMOS fabrication directly. Depending on the characteristic of the fabrication process, the variables for optimization include 2 variable that is heat transfer coefficient (x1) and optimal temperature (x2). About the variable x1, when deposition of last layer is complete, the CMOS-MEMS microphone will be cooled down to room temperature with different coefficient convective. The other variable, the temperature is chosen lower than room temperature and the CMOS-MEMS microphone will be returned to the room temperature later. Fig. 46 presents the design variable in the optimization process.

In this research, the simplified conjugate gradient method (SCGM) is used optimal currently CMOS fabrication process. Fig. 47 shows the variation of the objective function in the optimal process. It requires approximately 155 iterations to reach the optimal design. The Von Mises stress after finishing the CMOS fabrication process at room temperature is reduced from 291.8MPa to 277.8MPa. From the above illustrations, we demonstrate that the proposed method in this study is available to approach optimal result.

In addition, the relationship between variable and the iteration is discussed. The range of the variable x1 is $35W/m^2K < x1 < 50W/m^2K$ and variable x2 is $5^oC < x2 < 25^oC$. The optimization process is shown in Fig. 48. In here, the initial data is $x1 = 50W/m^2K$ and $x2 = 20^oC$ and these variables decrease after 155 iterations and converge with the value $x1 = 35W/m^2K$ and $x2 = 5^oC$. Through this figure, the variable x1 decreases nonlinear at the first time. After that, it transforms to decrease linearly. The variable x2 decreases very smooth and linear.

Fig. 49 presents the stress contour with the variation of heat transfer coefficient x1 and temperature x2 under room temperature. From the result of this figure, the minimum result is located in $x1 = 35W/m^2K$ and $x2 = 5^oC$ for minimization stress is equal to 277.8MPa.

On the other hand, the residual stress in each layer in initial CMOS fabrication and after optimization process is described in Figs. 50(a-g). As the result, the residual stress in all layers is reduced. The reduction gets maximum value at aluminum layer.

Specially, the maximum Von Mises stress profiles along the X-axis is shown in Fig. 51 under the initial design and optimization. Under the initial design, the stress concentration is very high and the peak stress is 291.8MPa. This is not only bad effect in the working but also reducing the lifetime of product. After the optimal procedure, the difference is 14MPa and the residual stress is reduced about 4.8%.

Moreover, Fig. 52 shows the residual stress distribution in initial CMOS fabrication process and the optimization. Through this figure, the residual stress distribution is very similar but high stress all decrease in each layer. It proves that the residual stress in CMOS fabrication process can minimum with suitable fabrication parameter.

3-5 Conclusion

The general purpose of the present study is used the ANSYS to predict the residual stresses during the CMOS fabrication. The coupled heat transfer and elastic – plastic finite element stress analyses were combined to simulate the generation of thermal stresses during CMOS fabrication process. The complicated physical fabrication process was idealized and a multiple layer by layer deposited structure was assumed. In the simulation, the geometry was updated layer by layer, the heat transfer and displacement is solved in the same time.

Besides, the “birth and death” method that is used on the analysis is validated by verifying the numerical results with previous paper. This means that the proposed method can simulate the real model effectively. In addition, it is found that birth and death method is a reliable and effective tool to estimate residual stress in CMOS fabrication process.

On other hand, a simple method by cooling under room temperature was also proposed to effectively reduce the residual stress level in the CMOS fabrication with the possibility of reducing the residual stress.

The extend application of ANSYS combine with SCGM are used to minimize residual stresses in CMOS fabrication process. The Von Mises stress is defined as object function to find the best valuable parameter in fabrication process. The heat transfer coefficient and optimal temperature after complete deposition is choose as variable to reduce residual stress. This means that suitable parameter fabrication can generate residual stress smaller in MEMS devices.

Table 7: Physical properties [35]

Material	Young's modulus (MPa)	Poison ratio	CTE	Free – stress temperature (^{0}K)
Silicon	129E3	0.28	2.62E-6	298
Thermal oxide	72E3	0.2	0.5E-6	1253
Polysilicon	169E3	0.22	2.3E-6	893
ILD	80E3	0.2	1.1E-6	1123
IMD	60E3	0.25	1.37E-6	673
Al	*Non - linear*	0.33	26E-6	773
Oxide (UGS)	60E3	0.25	1.37E-6	673
SiN	210E3	0.27	2E-6	673

Table 8: Thermal properties [35]

Material	Density (kg/m^3)	Specific heat capacity (J/kg*K)	Thermal conductivity (W/m*K)
Silicon	2329	700	130
Thermal oxide	2200	730	1.4
Polysilicon	2320	678	34
ILD	2320	678	34
IMD	3965	730	35
Al	2700	904	237
Oxide (UGS)	3965	730	35
SiN	3100	700	20

Table 9: The comparison between using ANSYS package and previous paper at 400^{o}C

X location	COMSOL	ANSYS with birth and death	Deviation (%)
-2.25E-04	-2.58E-07	-2.60E-07	0.78
-1.75E-04	-1.56E-07	-1.57E-07	0.64
-1.25E-04	-7.96E-08	-8.02E-08	0.75
-7.50E-05	-2.87E-08	-2.89E-08	0.70
-2.50E-05	-3.19E-09	-3.21E-09	0.63
0	0	0.00E+00	0.00
5.00E-05	-1.27E-08	-1.28E-08	0.75
1.00E-04	-5.10E-08	-5.13E-08	0.75
1.50E-04	-1.15E-07	-1.16E-07	0.75
2.00E-04	-2.04E-07	-2.05E-07	0.75
2.50E-04	-3.18E-07	-3.21E-07	0.75
			Average: 0.66

Table 10: The comparison between using ANSYS package and previous paper at 25^{o}C

X location	COMSOL	ANSYS with birth and death	Deviation (%)
-2.25E-04	6.49E-07	6.53E-07	0.62
-1.75E-04	3.92E-07	3.95E-07	0.77
-1.25E-04	2.00E-07	2.02E-07	1.00
-7.50E-05	7.21E-08	7.26E-08	0.69
-2.50E-05	8.01E-09	8.06E-09	0.62
0	0	0.00E+00	0.00
5.00E-05	3.20E-08	3.22E-08	0.69
1.00E-04	1.28E-07	1.29E-07	0.69
1.50E-04	2.88E-07	2.90E-07	0.69
2.00E-04	5.12E-07	5.16E-07	0.69
2.50E-04	8.00E-07	8.06E-07	0.69
			Average: 0.59

Table 11: The comparison between method with and without birth and death at 25^{o}C

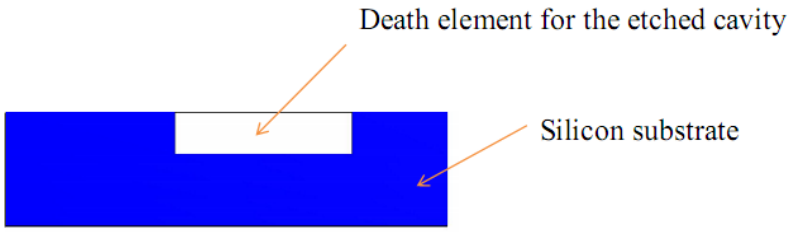
X location	ANSYS without birth and death	ANSYS with birth and death	Deviation (%)
-2.25E-04	3.88E-07	6.53E-07	68.29
-1.75E-04	2.35E-07	3.95E-07	68.28
-1.25E-04	1.20E-07	2.02E-07	68.67
-7.50E-05	4.31E-08	7.26E-08	68.40
-2.50E-05	4.79E-09	8.06E-09	68.26
0	0	0.00E+00	0.00
5.00E-05	1.92E-08	3.22E-08	68.30
1.00E-04	7.66E-08	1.29E-07	68.30
1.50E-04	1.72E-07	2.90E-07	68.30
2.00E-04	3.07E-07	5.16E-07	68.30
2.50E-04	4.79E-07	8.06E-07	68.29
			Average: 55.92

Table 12: Detail simulation

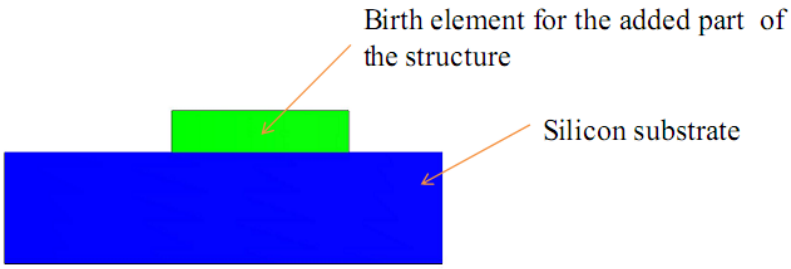
Parameter	Application modes			Step
	1st Layer	2nd Layer	…	
Material *Temperature* Temp reference	***Death element***	***Death element***	…	…
Material *Temperature* Temp reference	***Death element***	**Polysilicon** 850^0C 620^0C	…	3
Material *Temperature* Temp reference	**SiO_2** 620^0C 980^0C	**SiO_2** 850^0C 980^0C	…	2
Material *Temperature* Temp reference	**Si** 620^0C 980^0C	**Si** 850^0C 980^0C	…	1

Table 13: Comparison of the residual stress in three cases

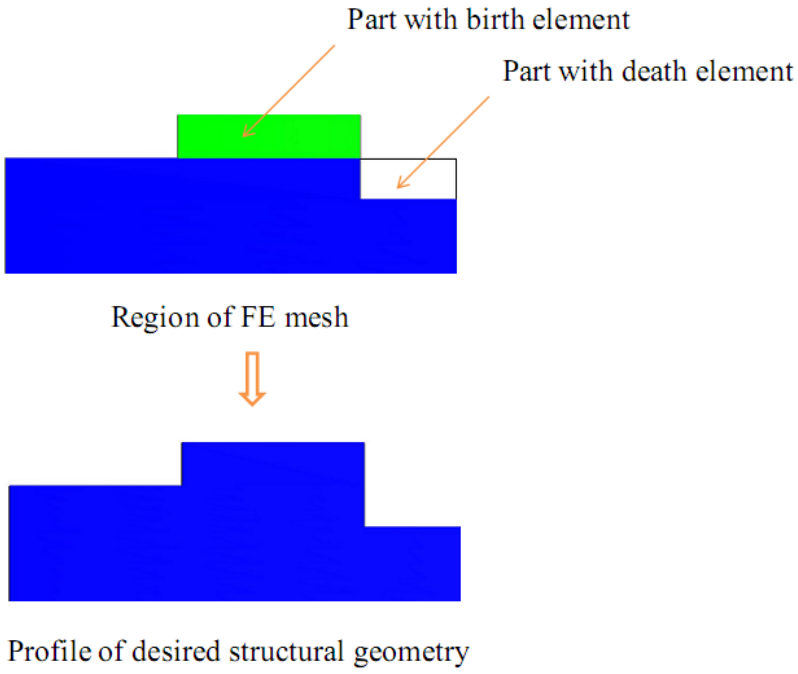
Case	Stress Sx		Stress Sy		Shear stress Sxy	
	Compress	Tensile	Compress	Tensile	Compress	Tensile
A	-216.1	257.5	-123.8	111.1	-96	70.9
B	-211.1	246	-116.8	110	-92.4	67.8
C	-205.9	234.5	-109.9	108.9	-88.8	64.7



a. Death element in etching process.



b. Birth element in deposition process.



c. Combine birth and death element in micro fabrication.

Fig. 22: Birth and death element application in micro fabrication

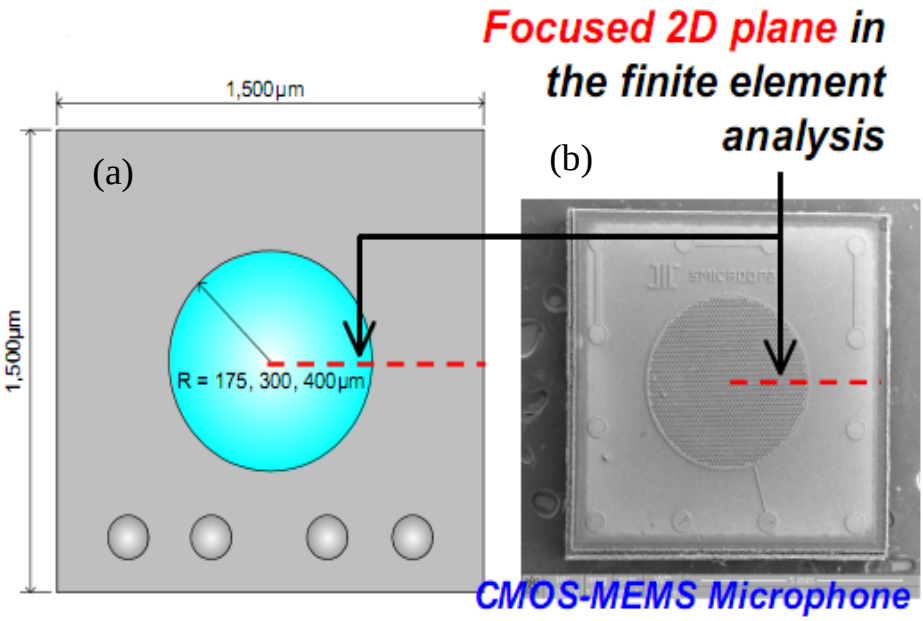


Fig. 23: (a) The illustration and (b) SEM picture of CMOS-MEMS Microphone

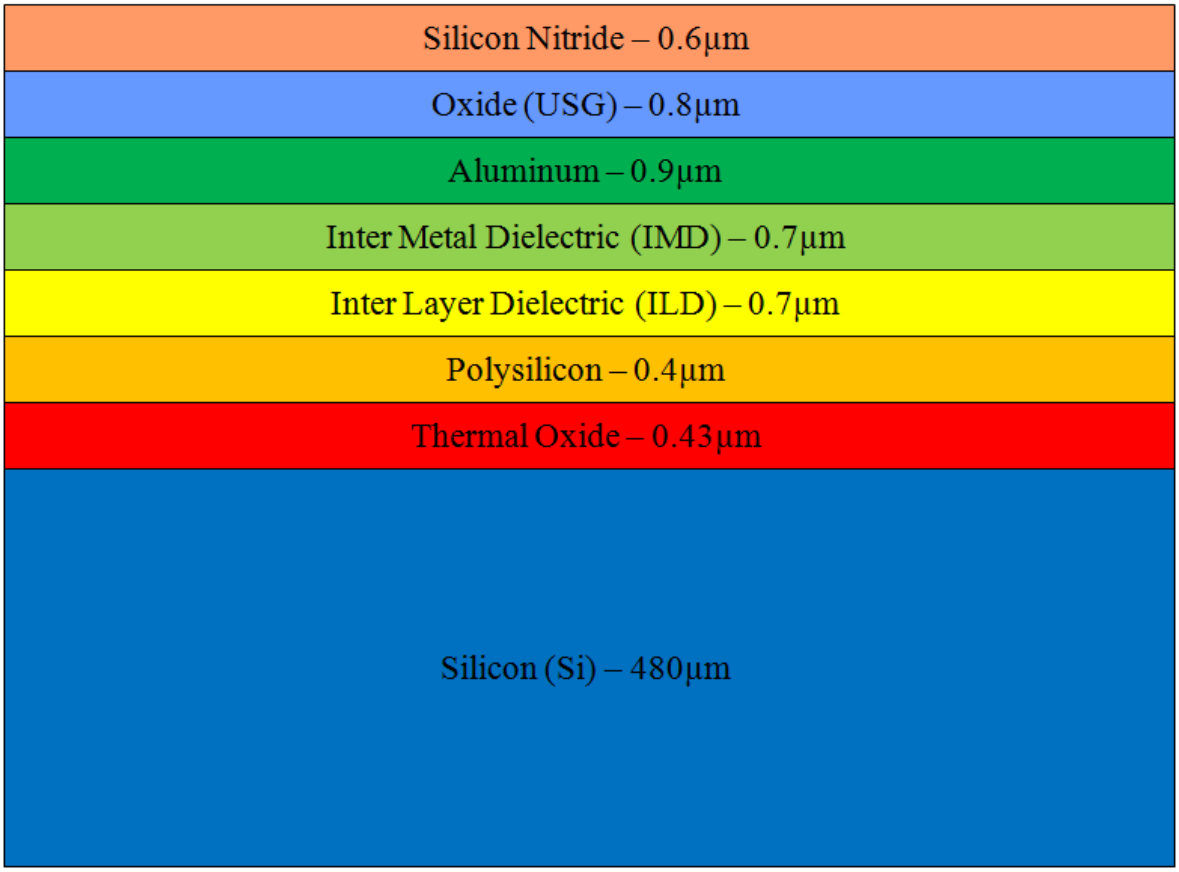


Fig. 24: Simplified coess-section of CMOS – MEMS Microphone

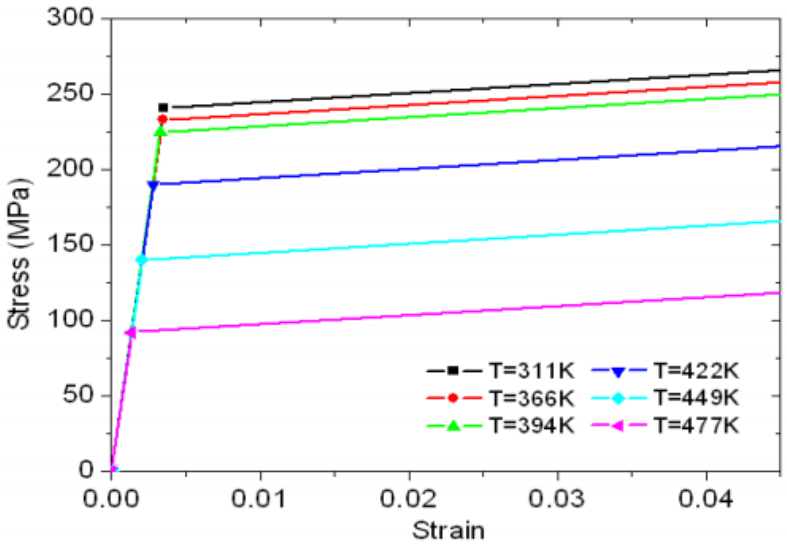


Fig. 25: Bilinear hardening behavior of Aluminum

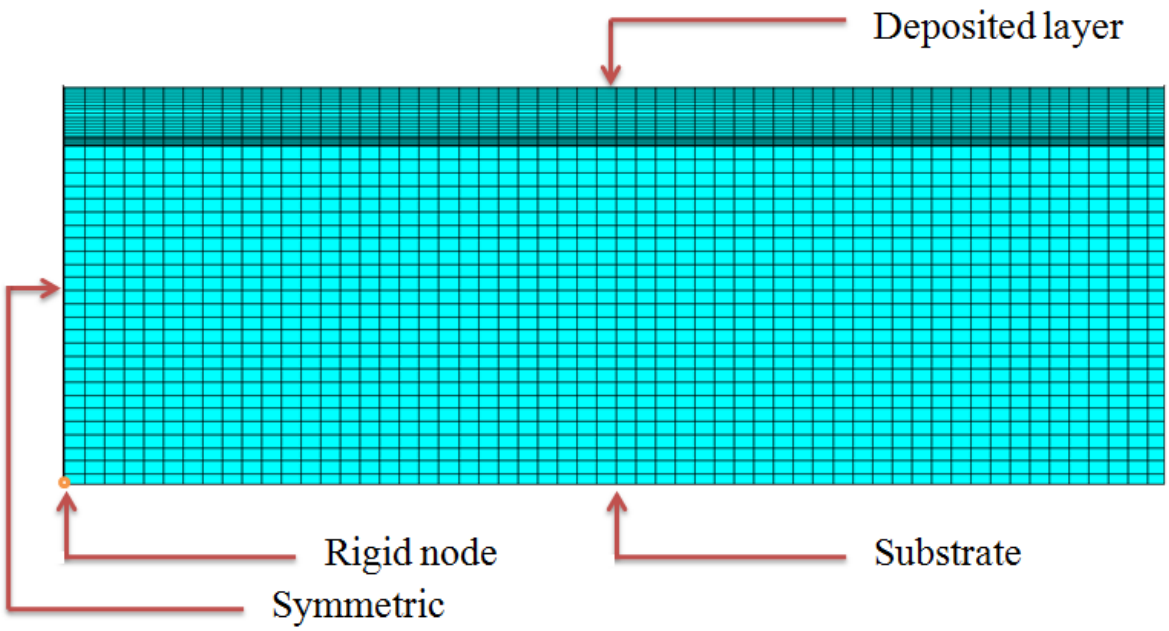


Fig. 26: Physical boundary conditions applied in model

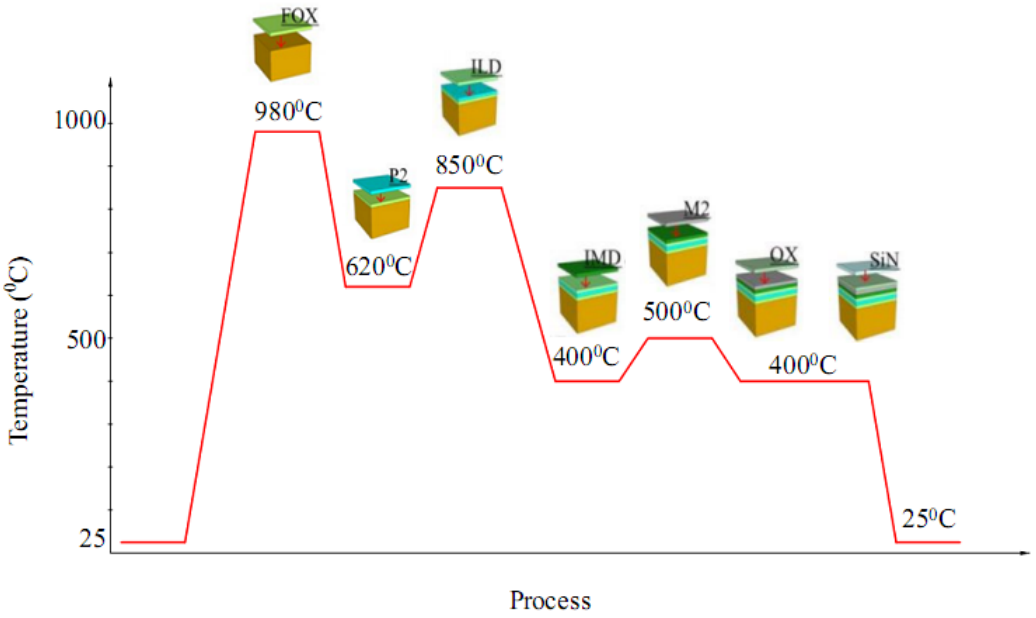


Fig. 27: CMOS fabrication process

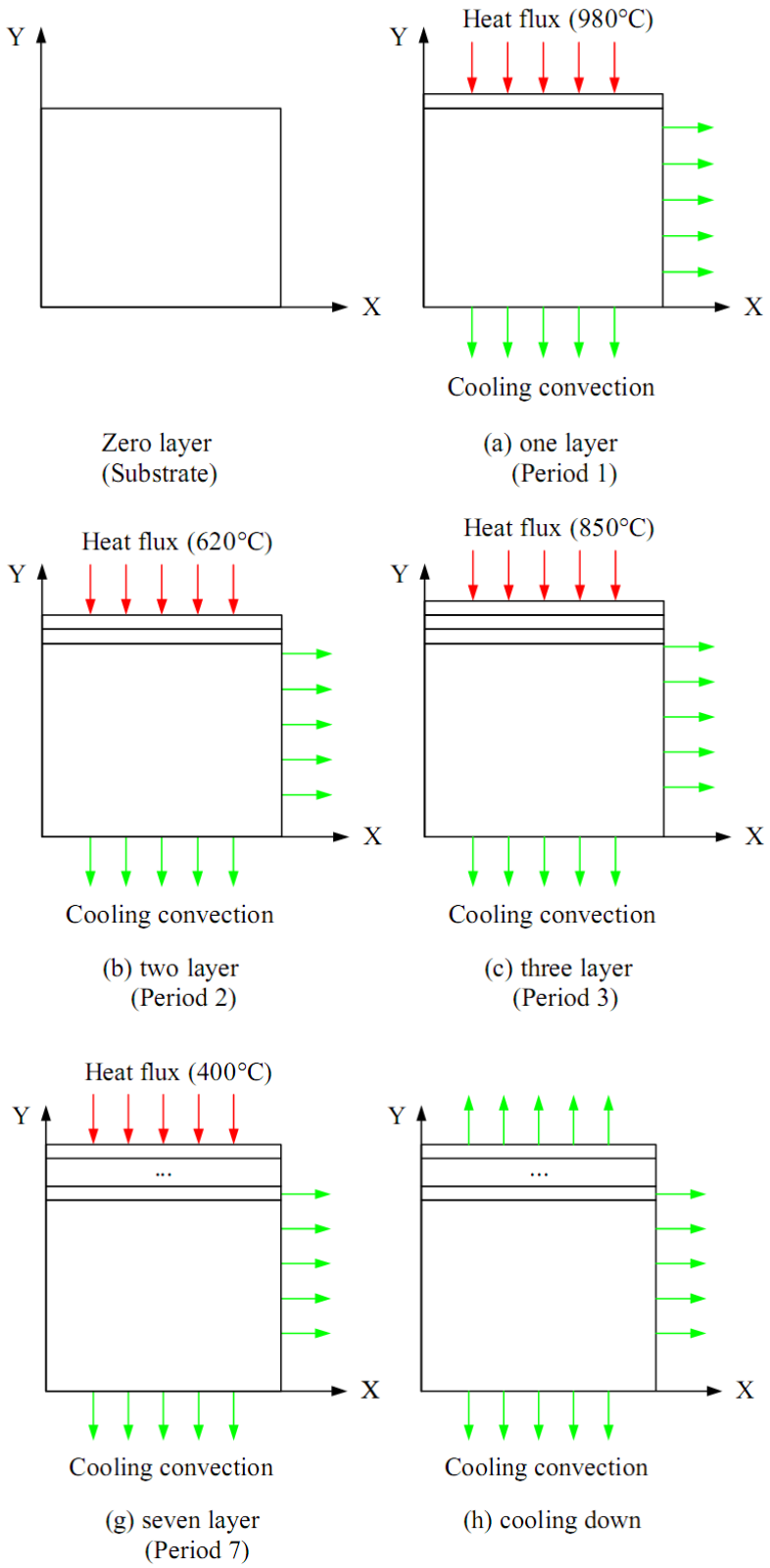


Fig. 28: Boundary condition for heat transfer with continuous updating of the geometry

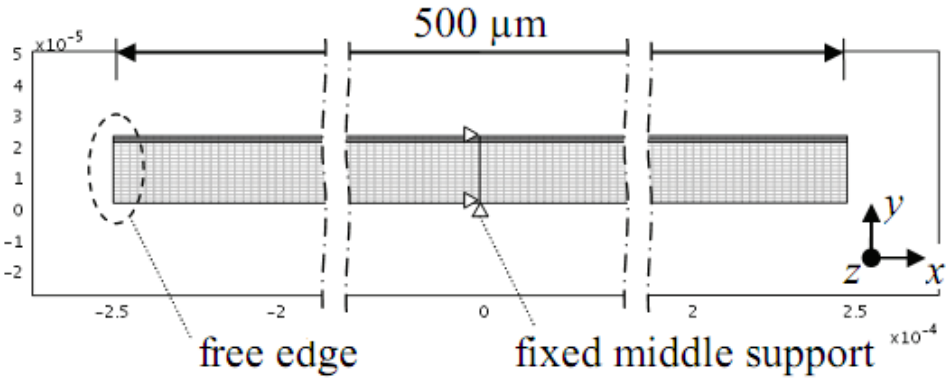


Fig. 29: Model and constraint, H. Conrad et al.’s study [57]

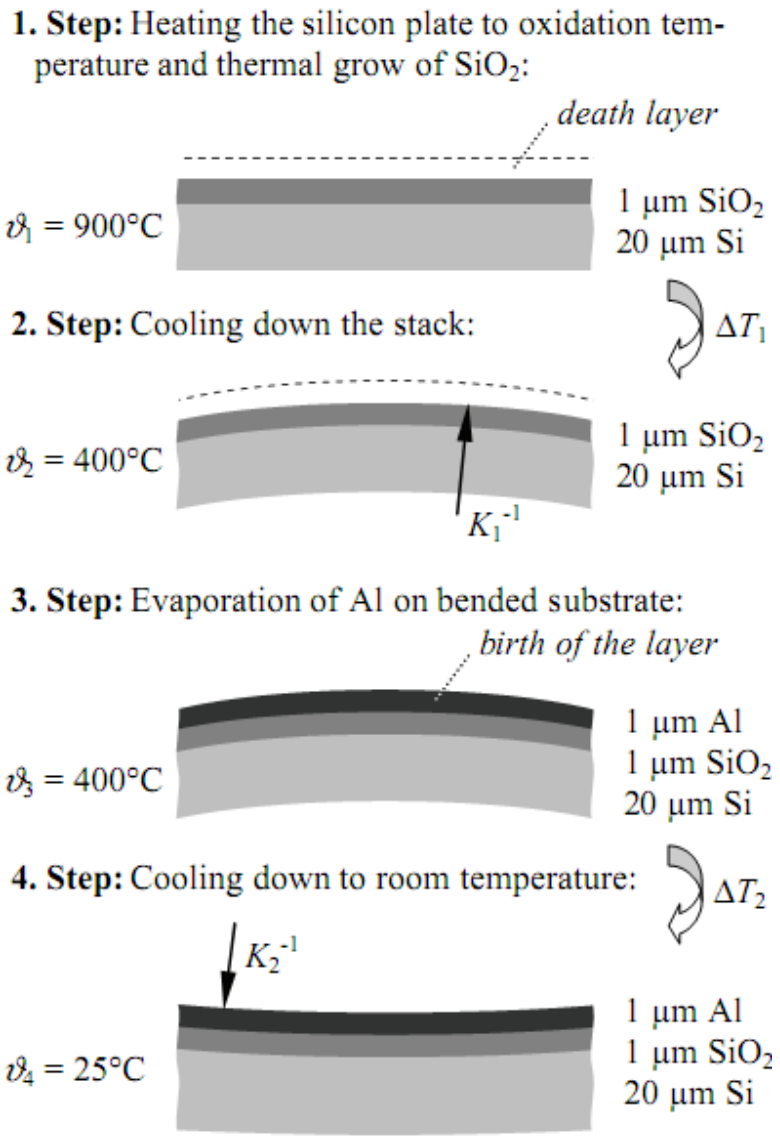
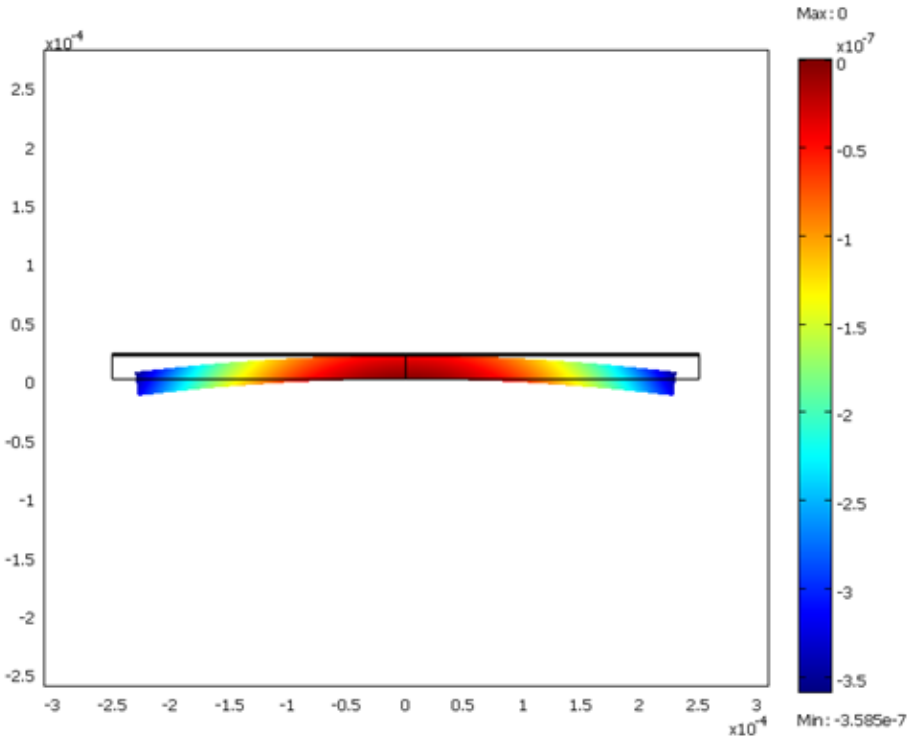
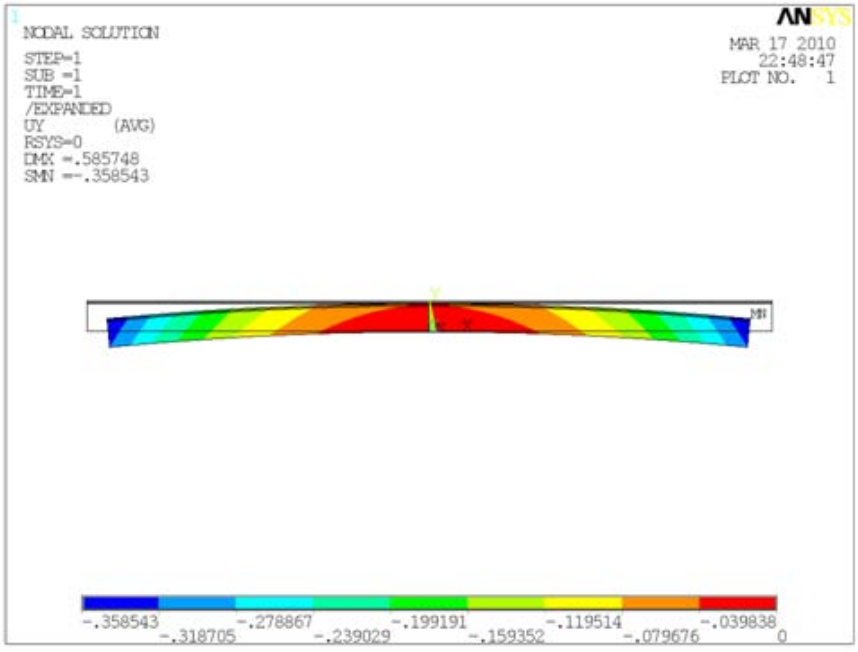


Fig. 30: Process and boundary condition, H. Conrad et al.'s study [57]



a. H. Conrad et al.'s study [57] at 400°C



b. Present study at 400°C

Fig. 31: Y displacement at 400°C in the validation

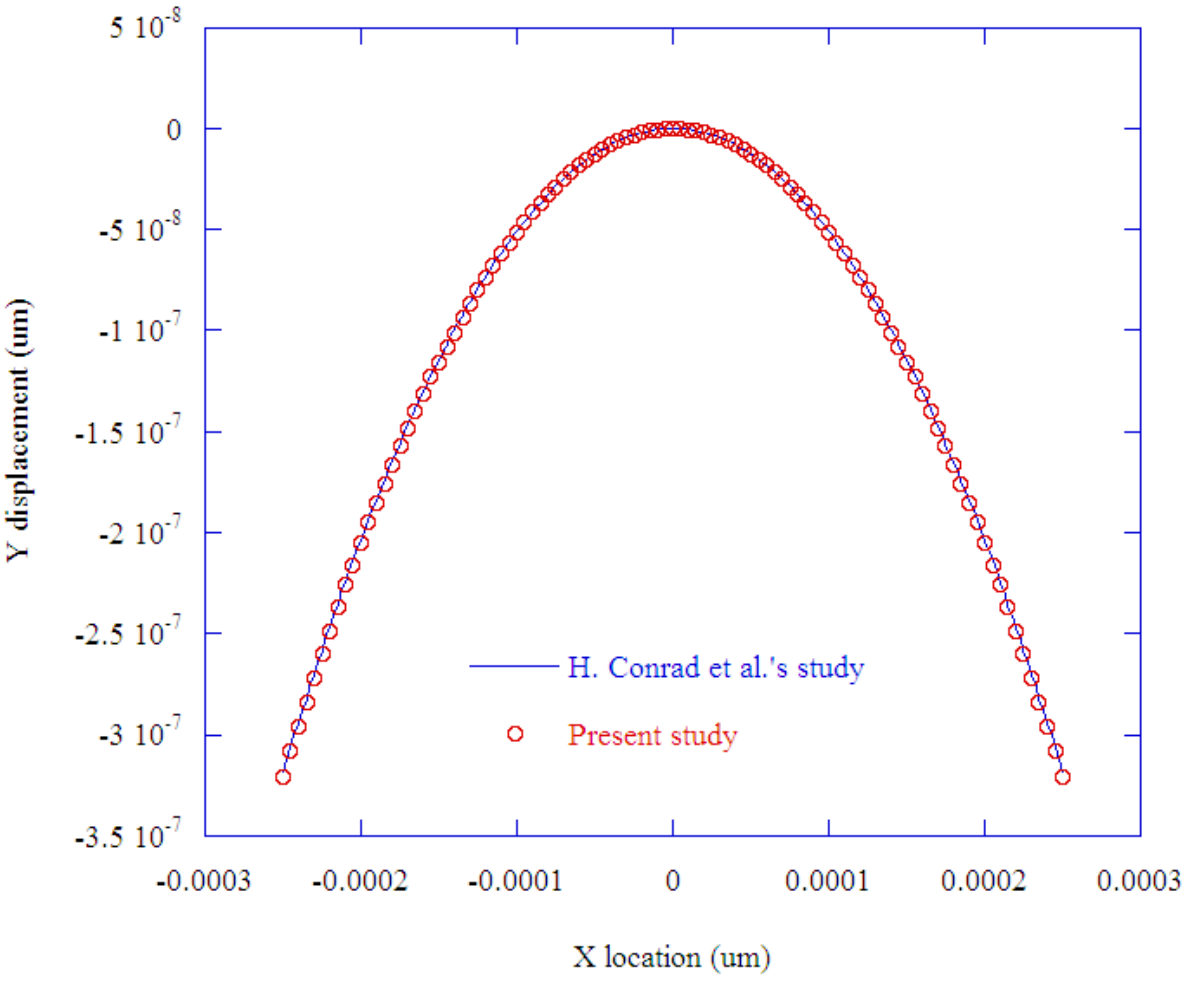
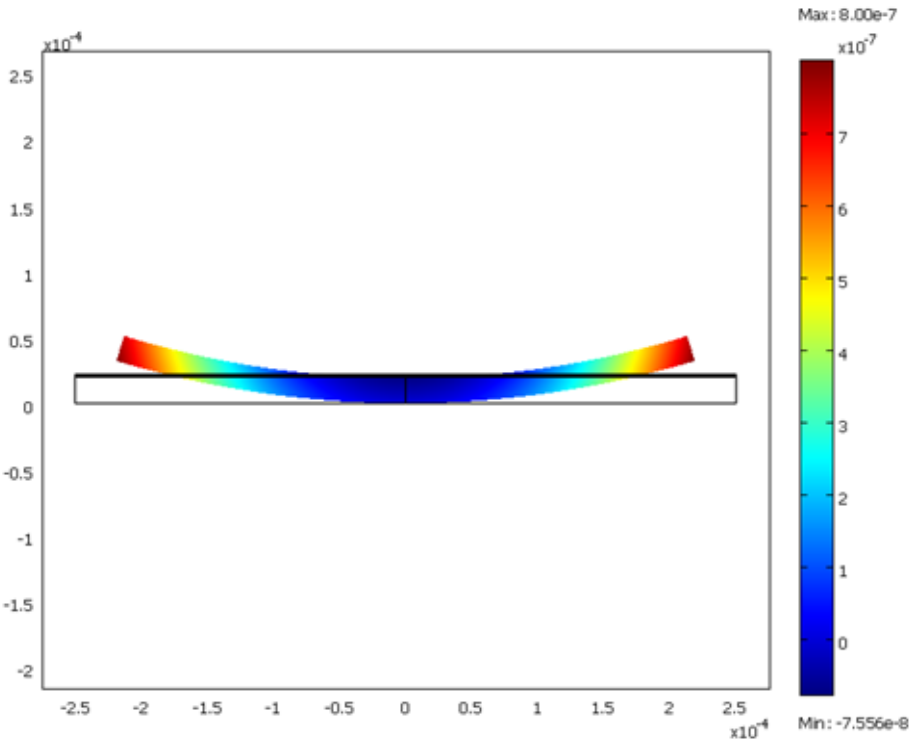
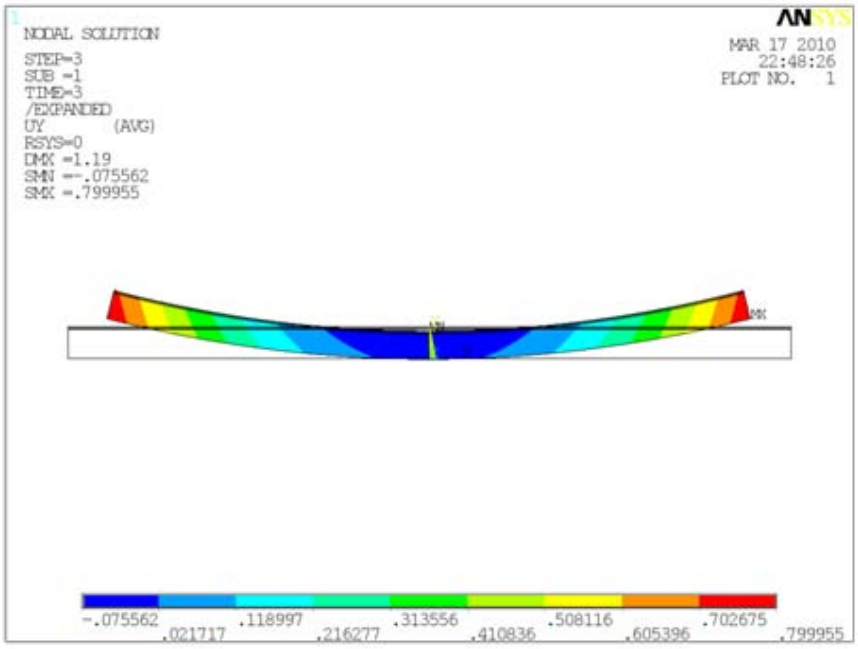


Fig. 32: The comparison of the surface deformation after deposition SiO_2 layer at 400^{o}C



a. H. Conrad et al.'s study [57] at 25°C



b. Present study at 25°C

Fig. 33: Y displacement at 25°C in the validation

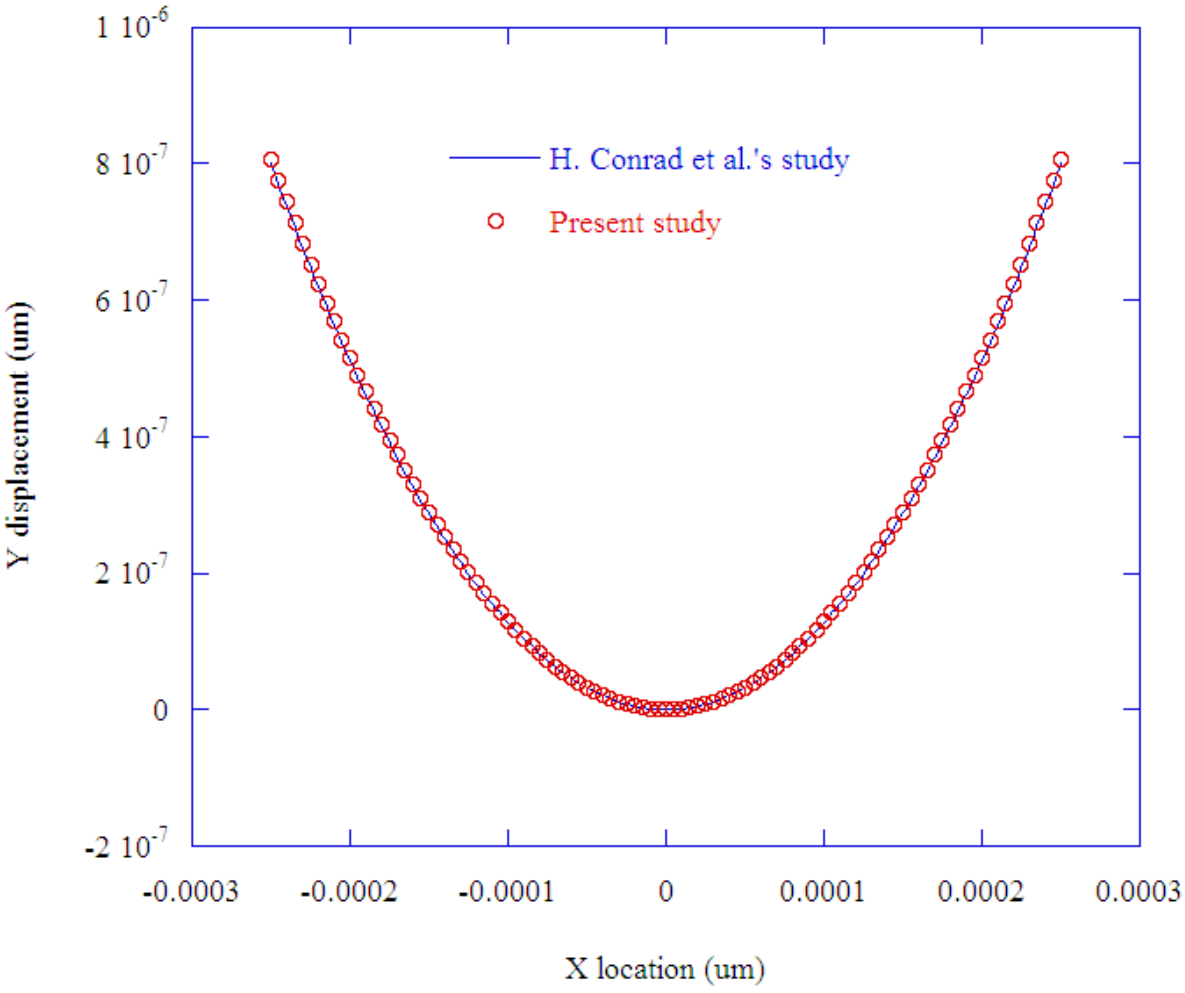


Fig. 34: The comparison of the surface deformation after deposition Al layer at 25^{o}C

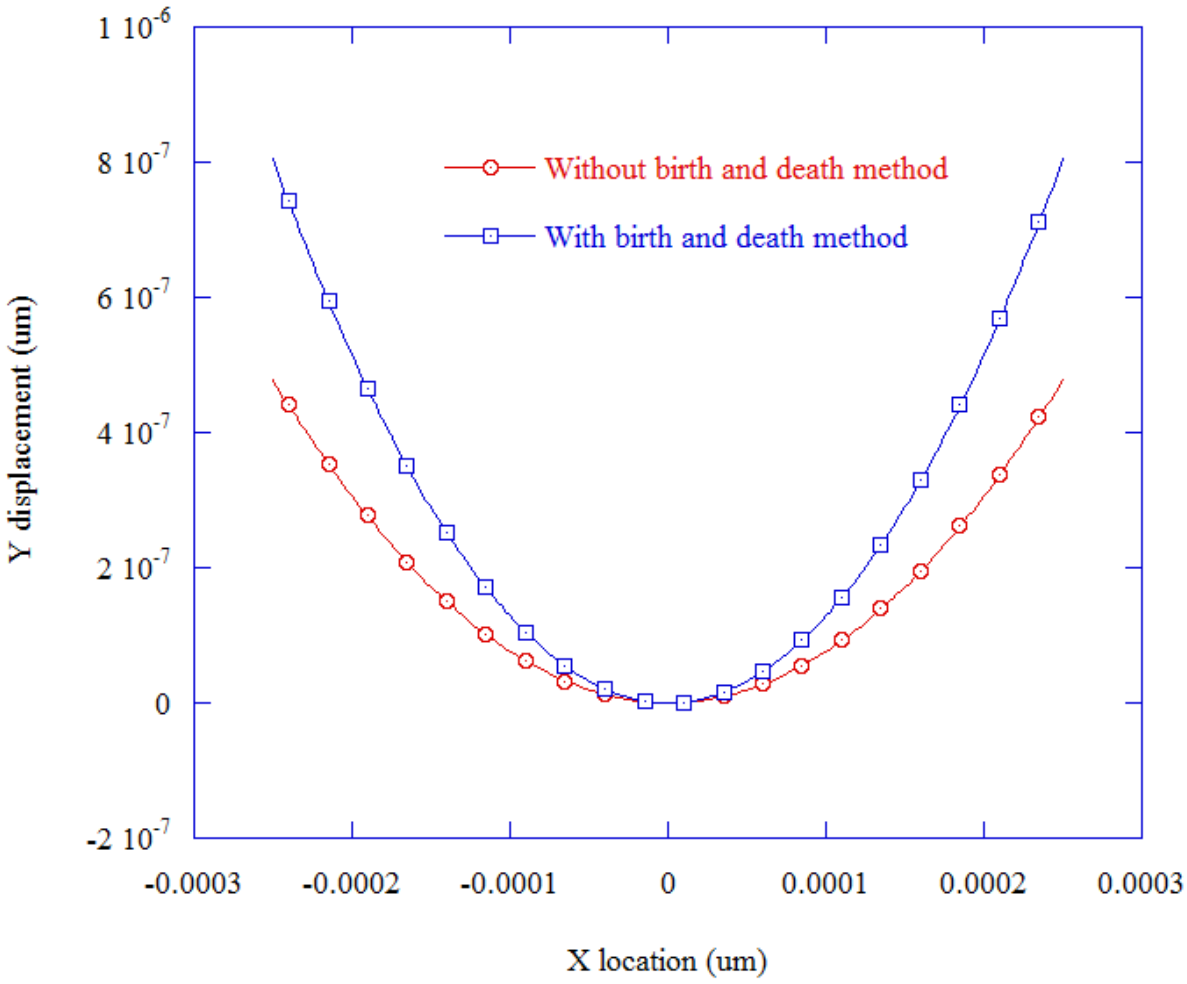


Fig. 35: The comparison of the surface deformation between method with and without birth and death element at 25^{o}C

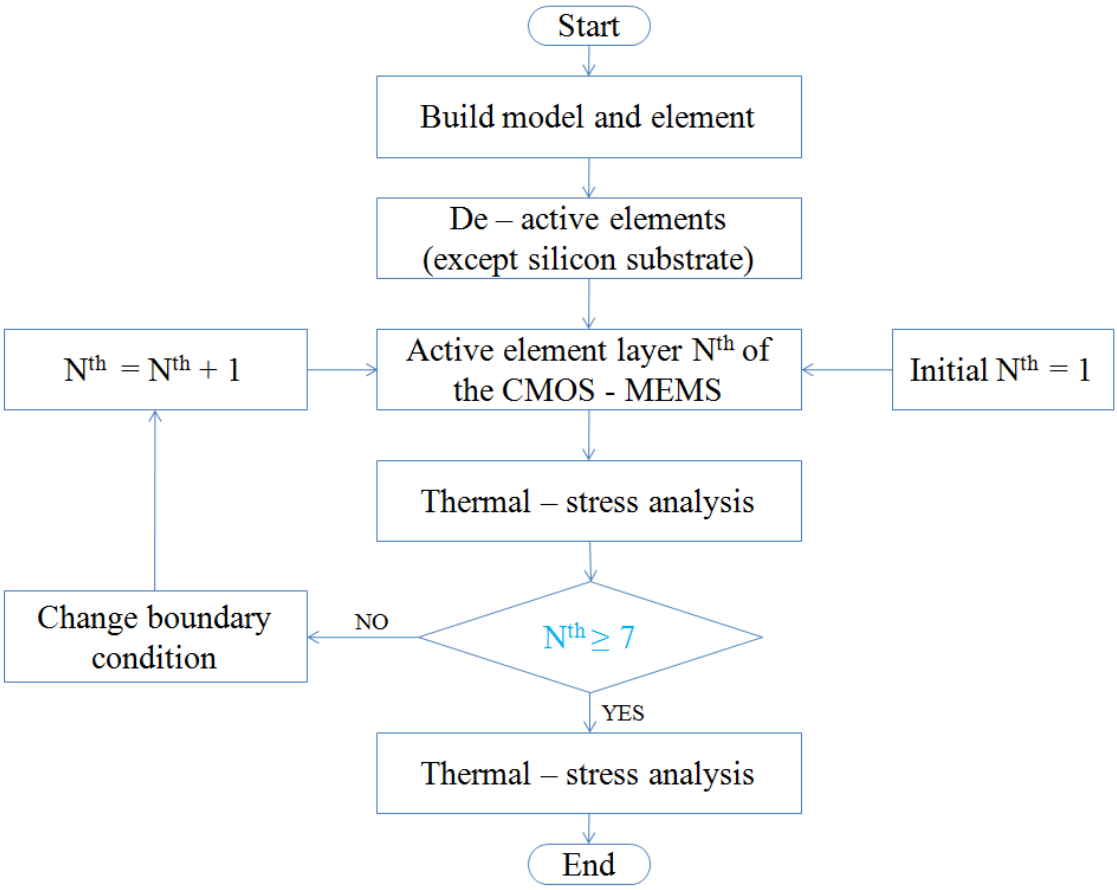


Fig. 36: Flowchart describes simulation methodology

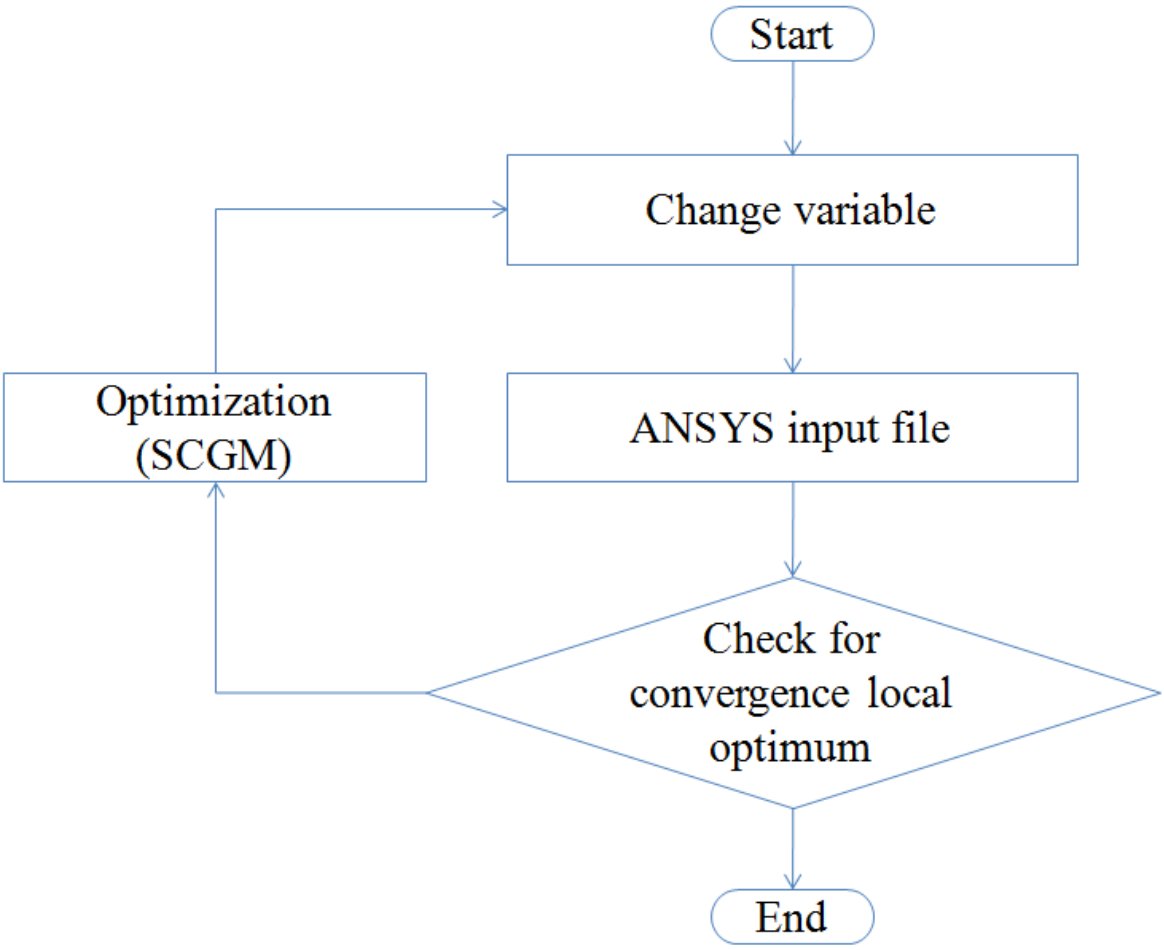


Fig. 37: The optimal process follows steps of the flow chart

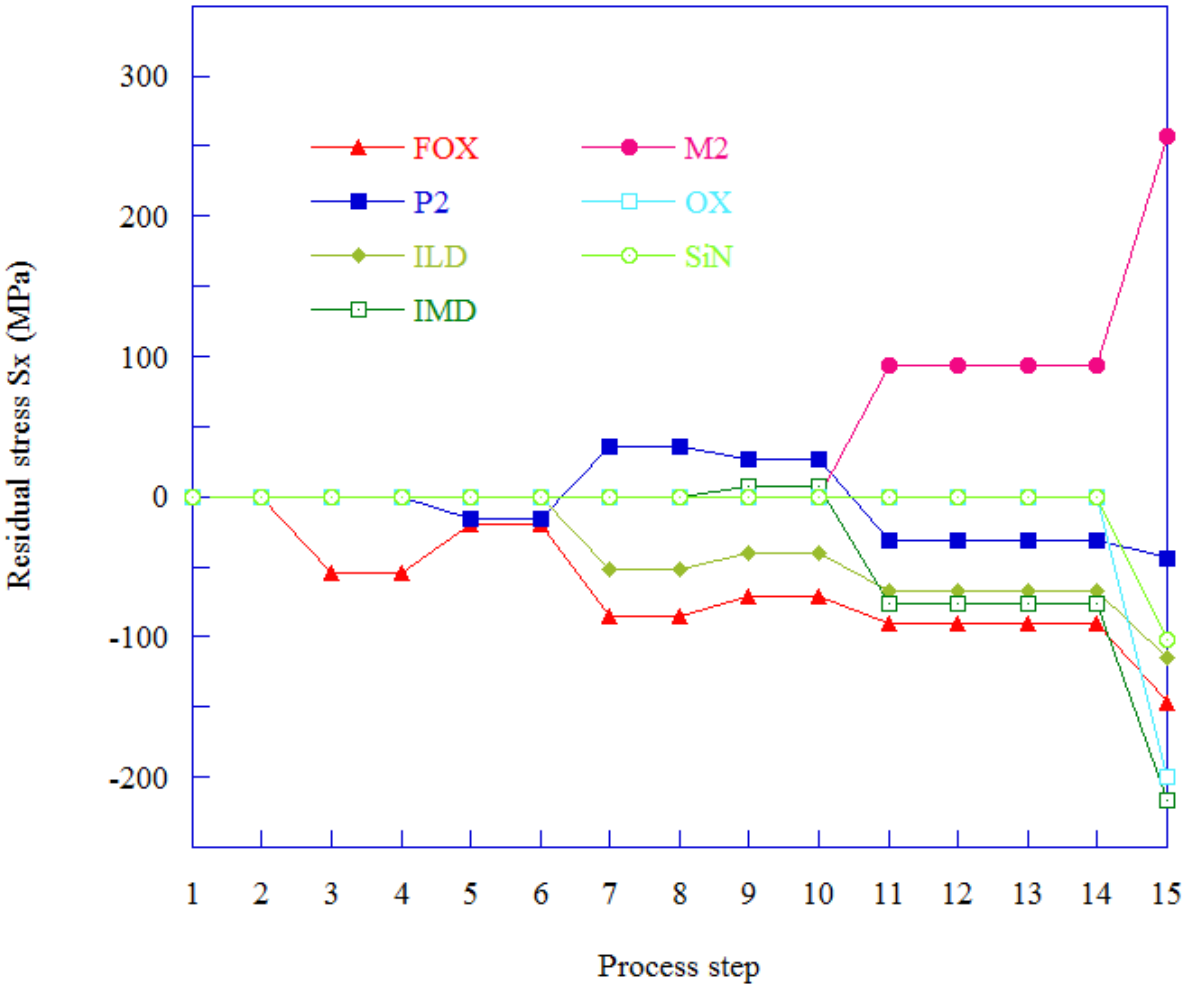


Fig. 38: Stress variation during fabrication process steps in different thin film

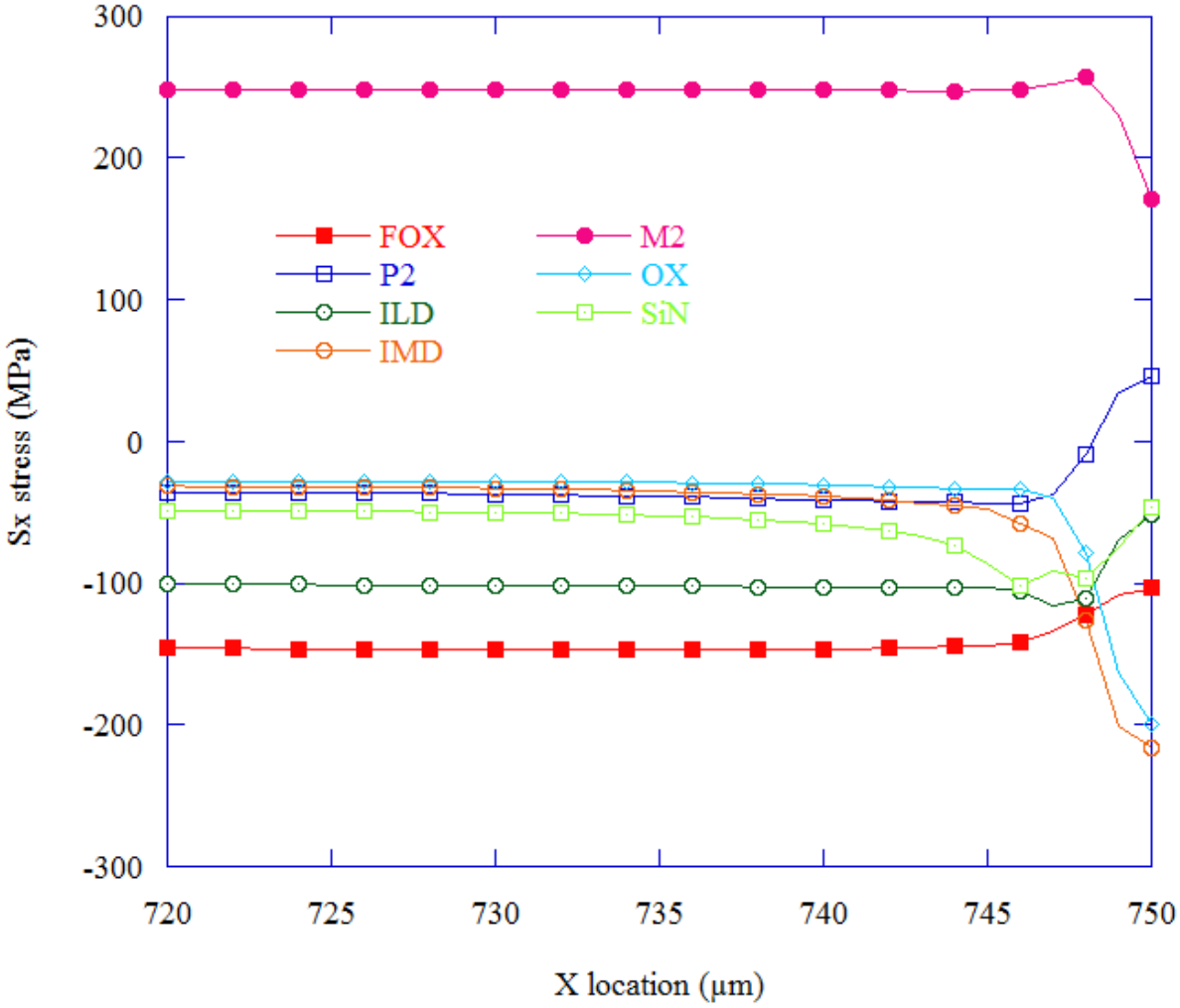


Fig. 39: Sx through the length of symmetric CMOS in each layer

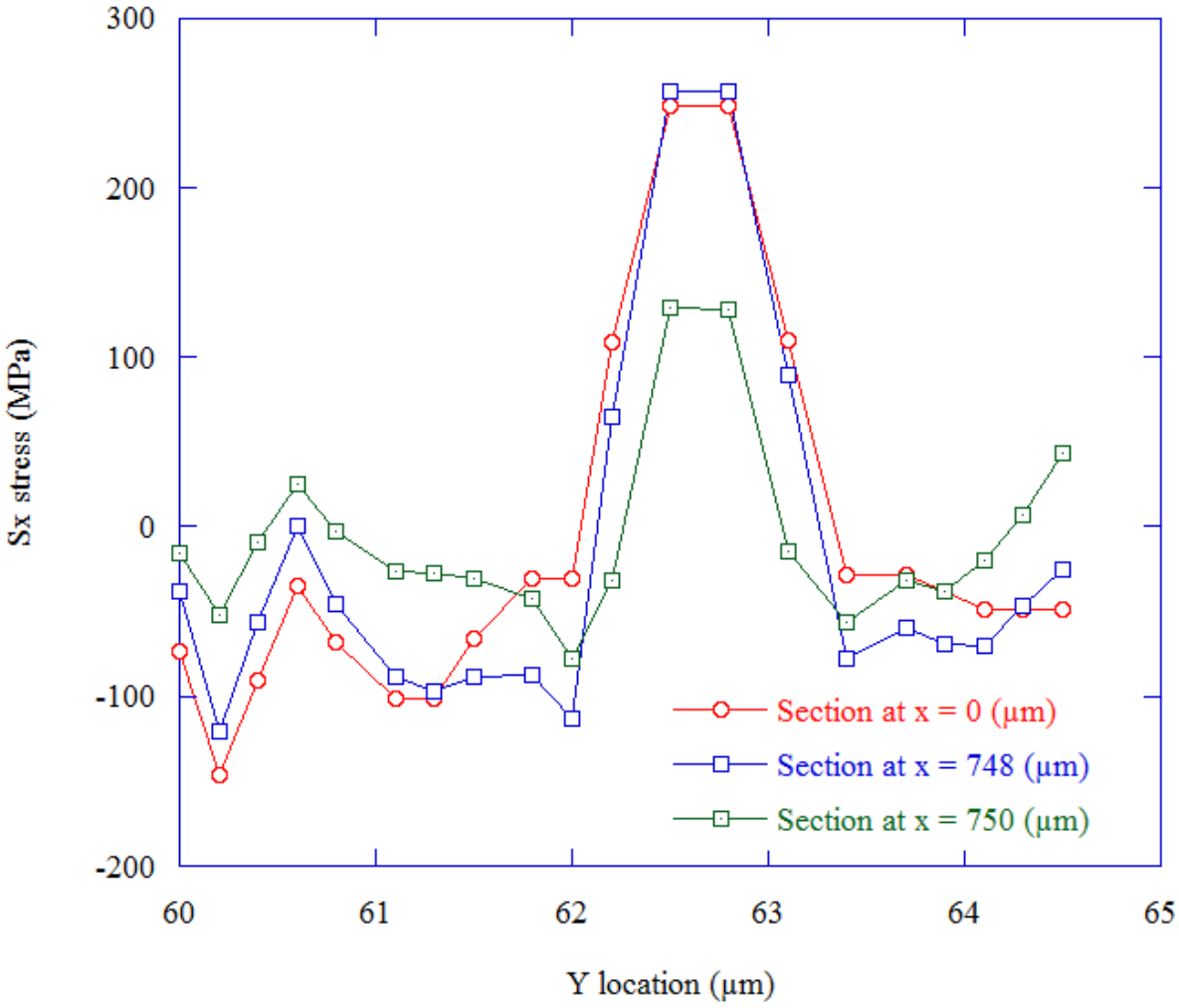
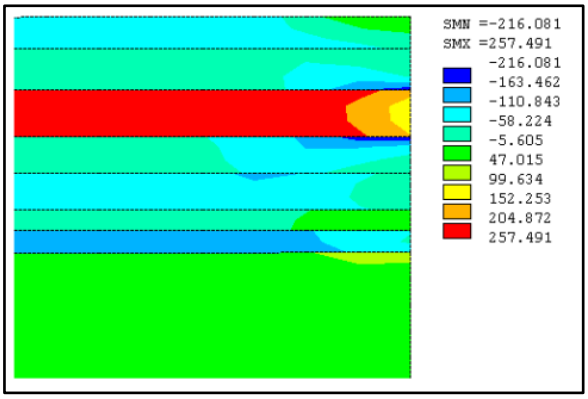
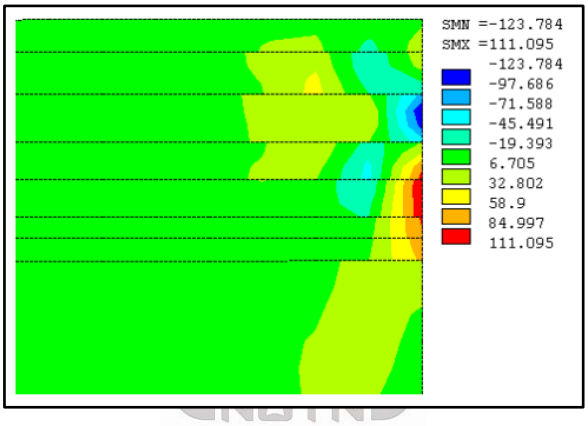


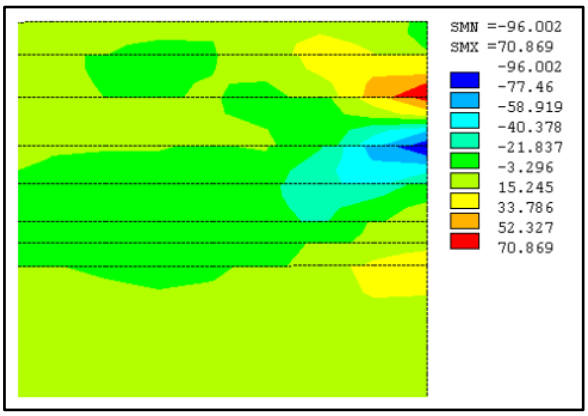
Fig. 40: Sx stress follows section at different x location



a. Sx distribution



b. Sy distribution



c. Sxy distribution

Fig. 41: (a) Sx, (b) Sy and (c) Sxy distribution of simplified CMOS fabrication process at room temperature

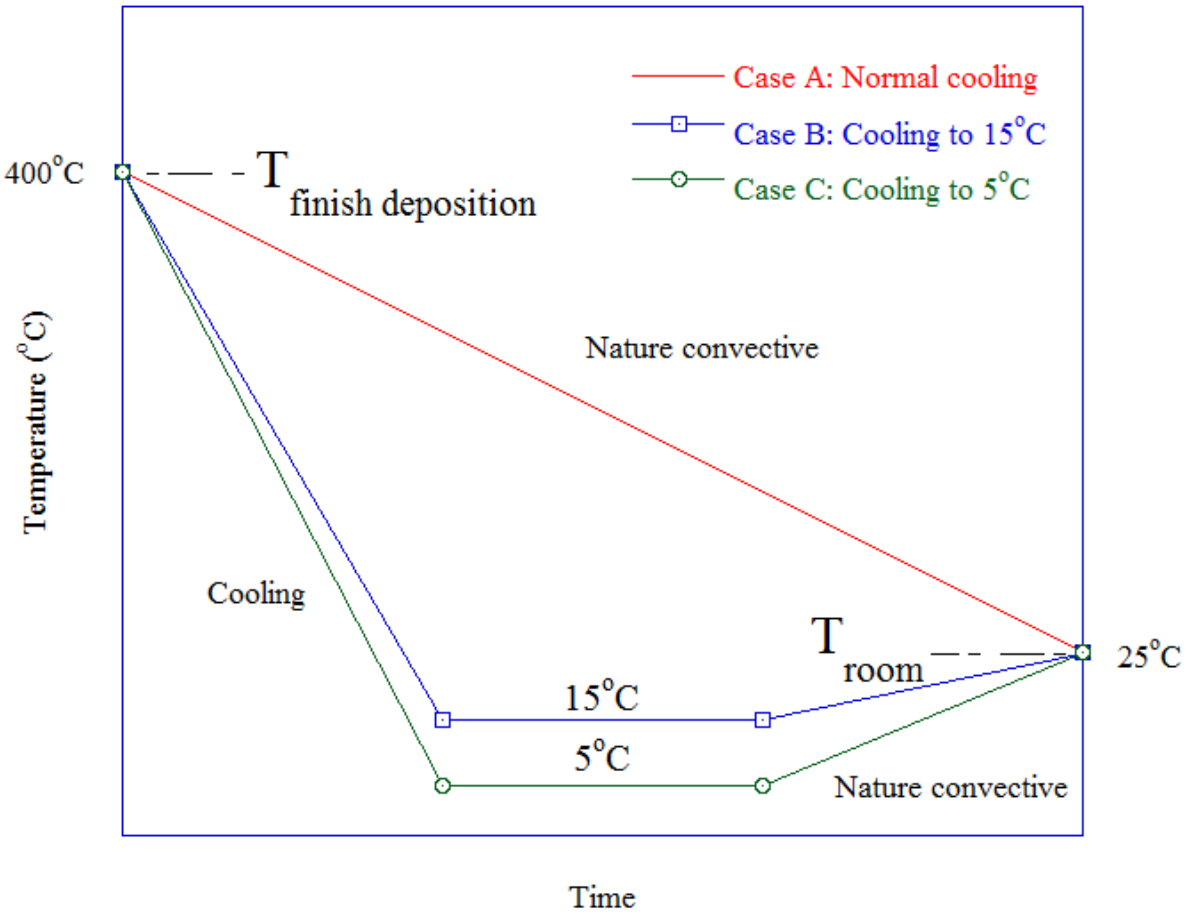
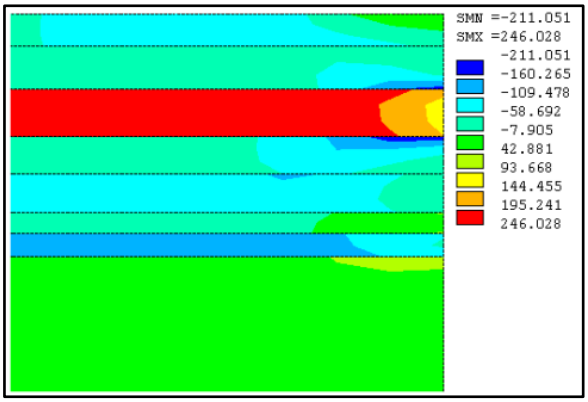
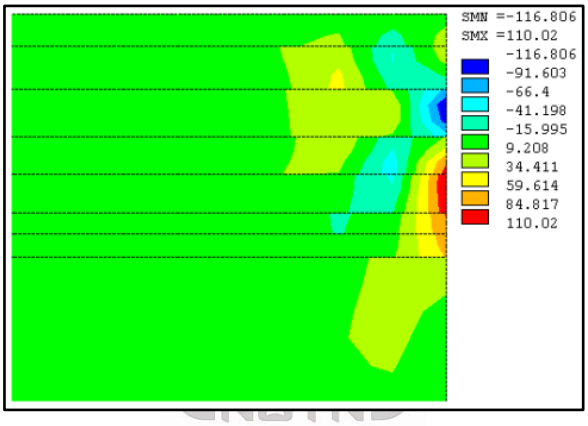


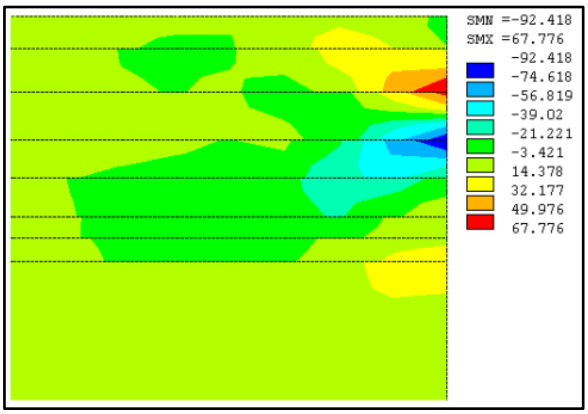
Fig. 42: Three cases studied to reduce the residual stress



a. Sx distribution

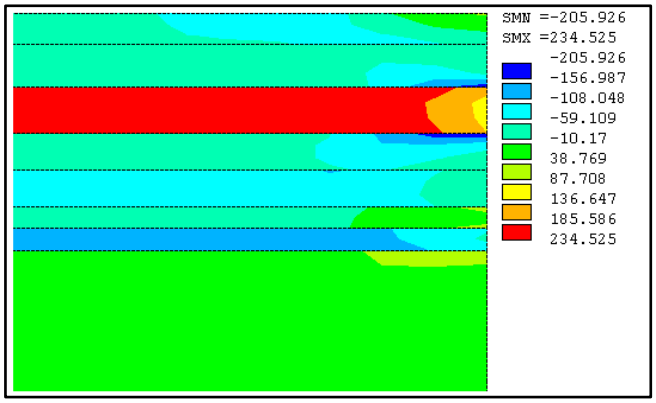


b. Sy distribution

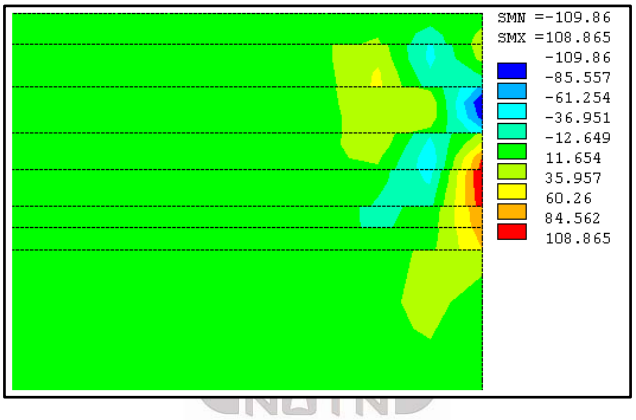


c. Sxy distribution

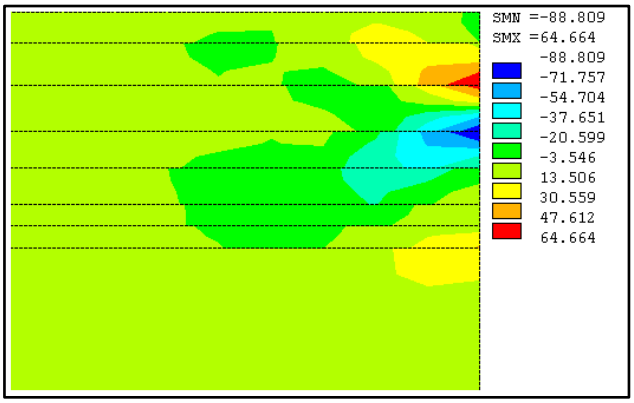
Fig. 43: (a) Sx, (b) Sy and (c) Sxy distribution of simplified CMOS fabrication process at room temperature in case B



a. Sx distribution



b. Sy distribution



c. Sxy distribution

Fig. 44: (a) Sx, (b) Sy and (c) Sxy distribution of simplified CMOS fabrication process at room temperature in case C

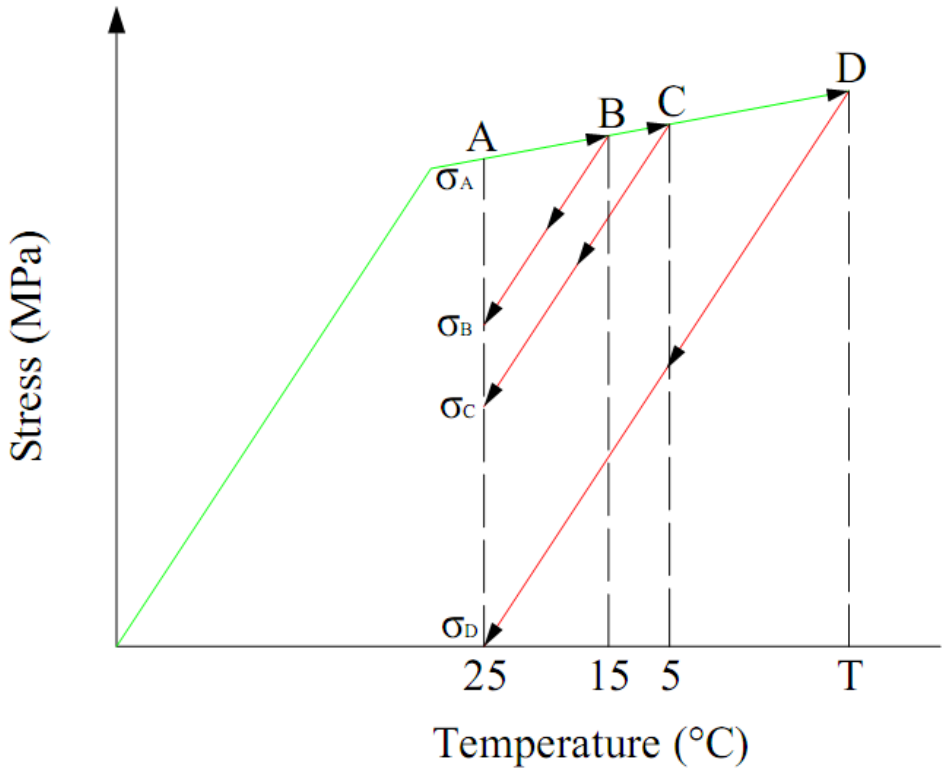


Fig. 45: Schematic constitutive model for cases A, B, C

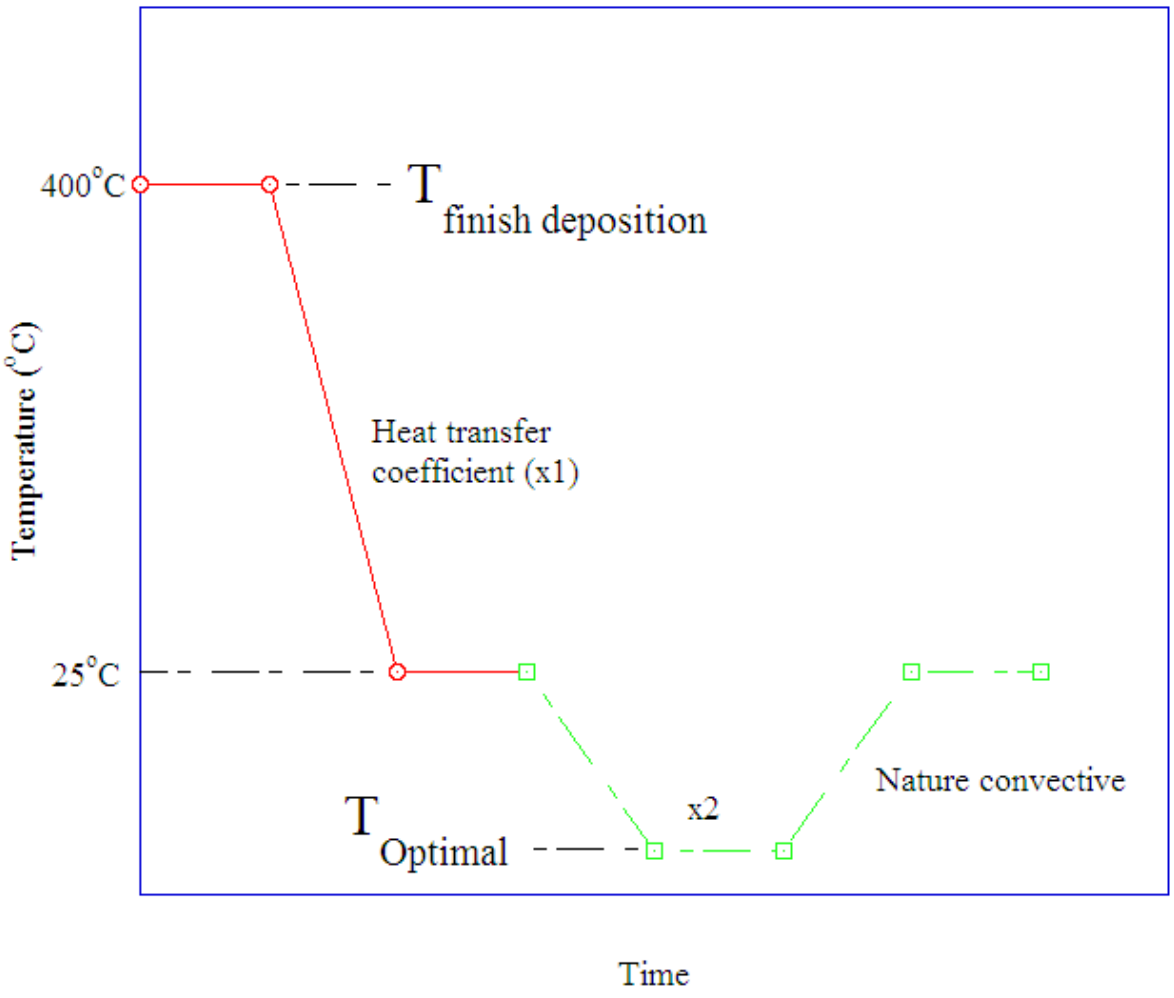


Fig. 46: Choosing variable for optimization

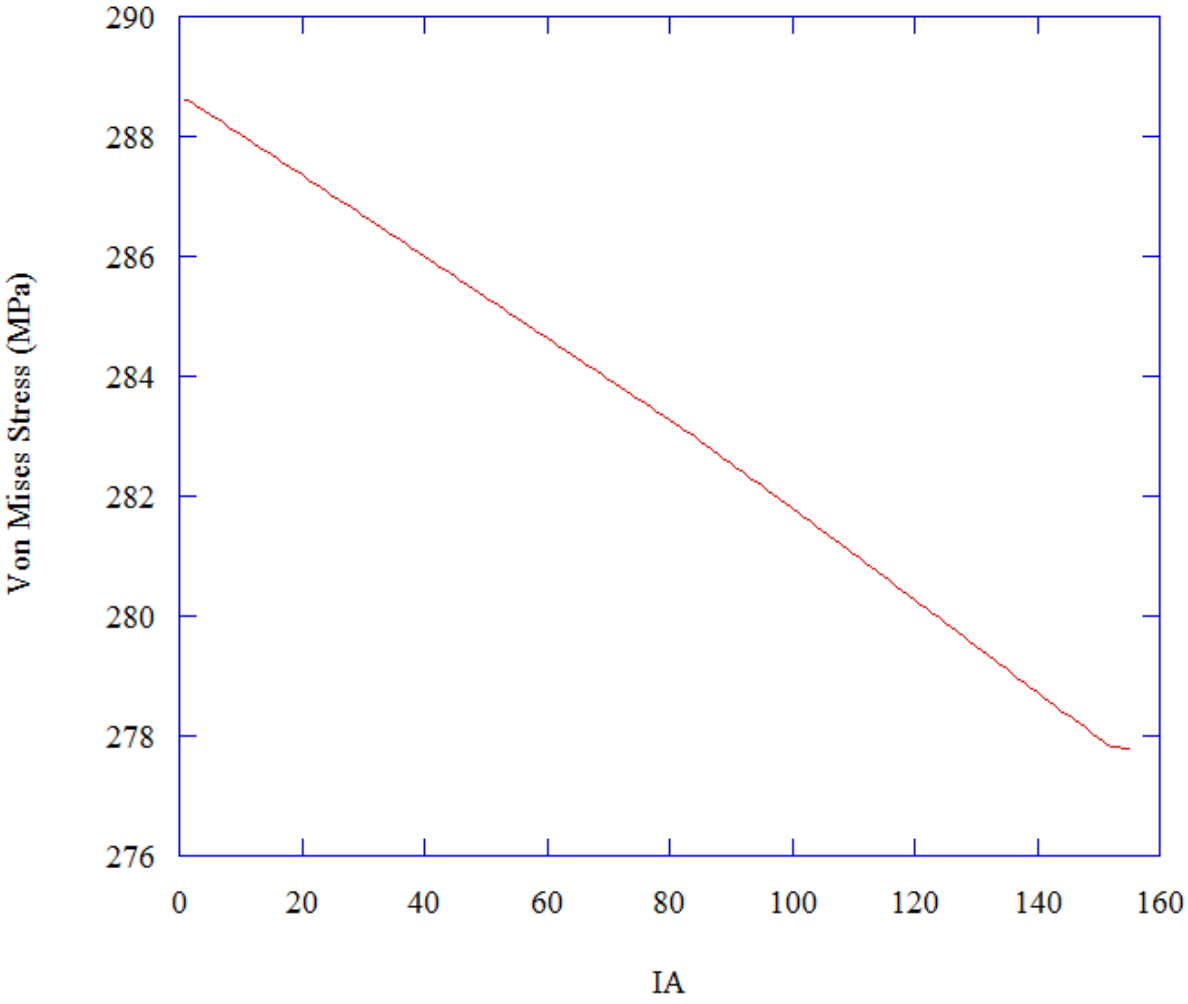


Fig. 47: The variation of the objective function in the optimal process

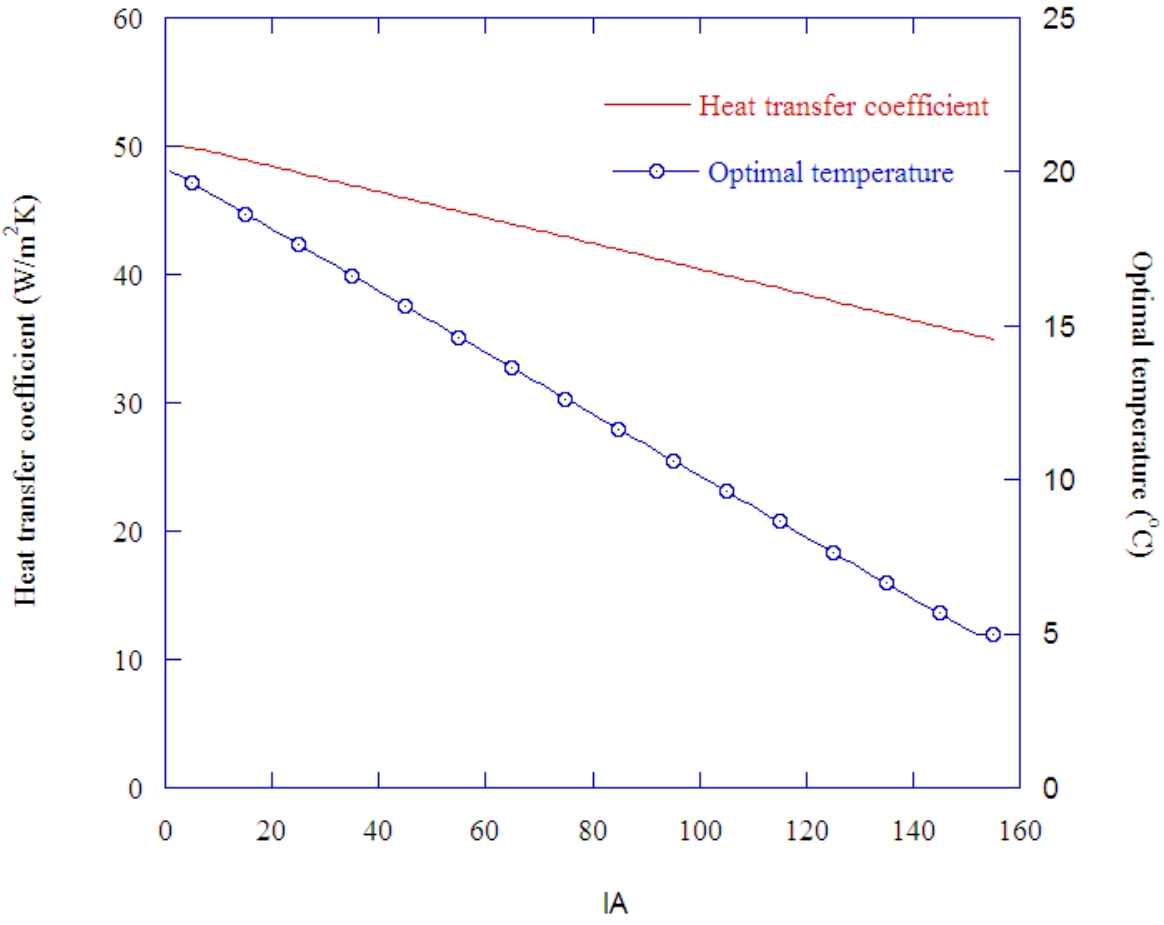


Fig. 48: The relationship between iteration and variable in optimization

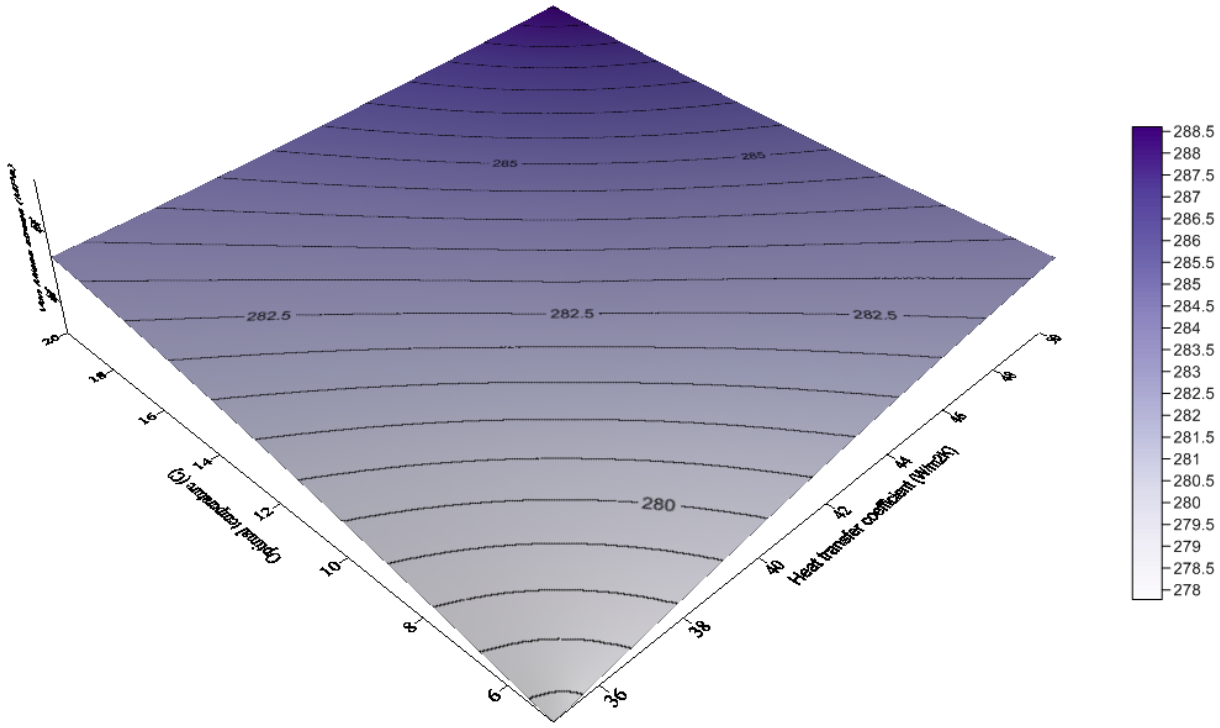
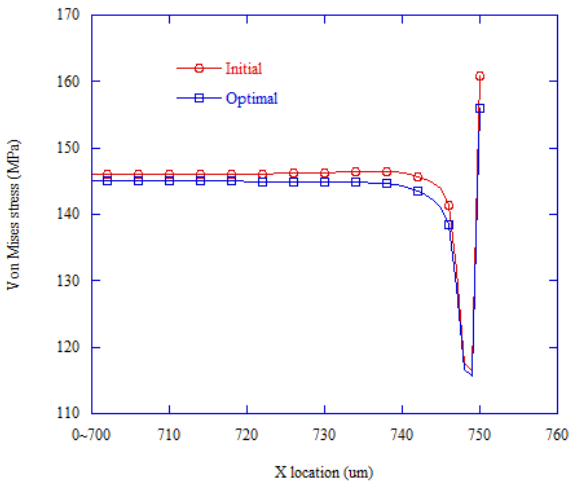
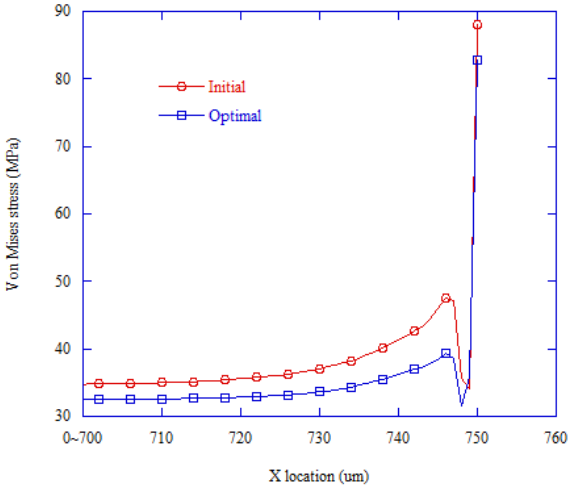


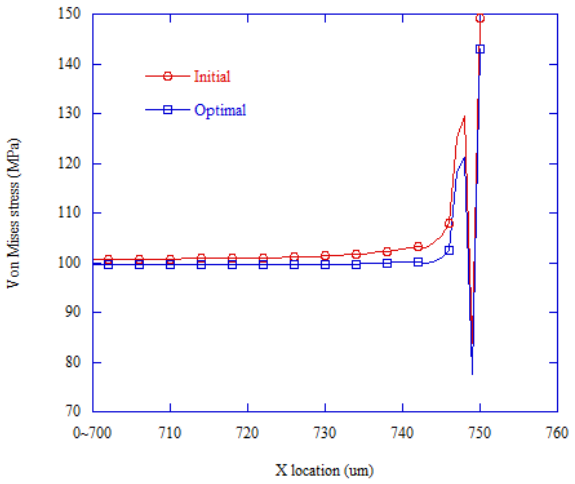
Fig. 49: The result optimal process CMOS fabrication



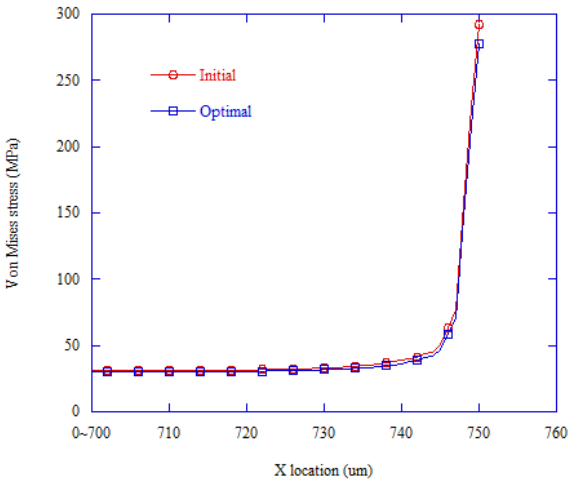
a. Thermal oxide layer



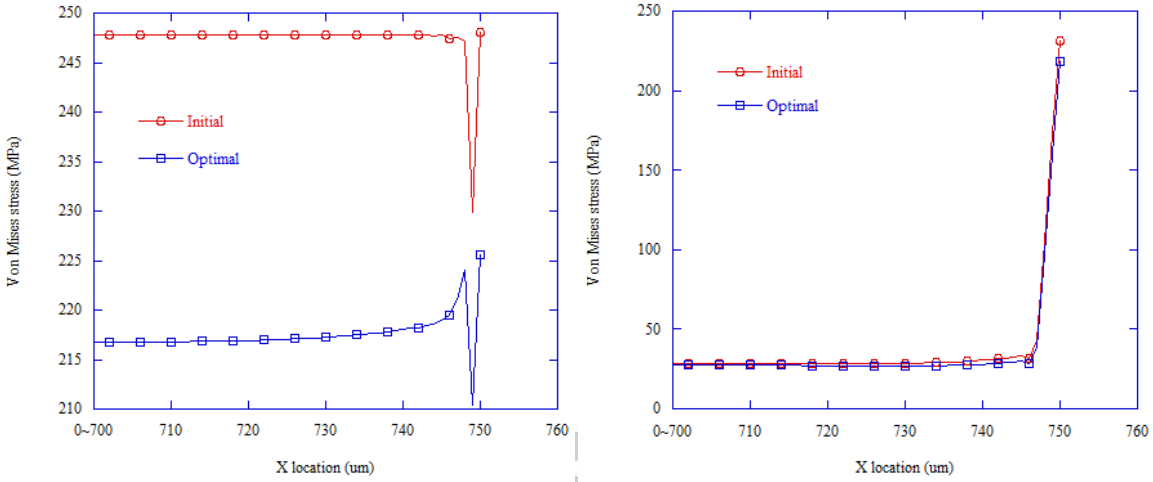
b. Polysilicon layer



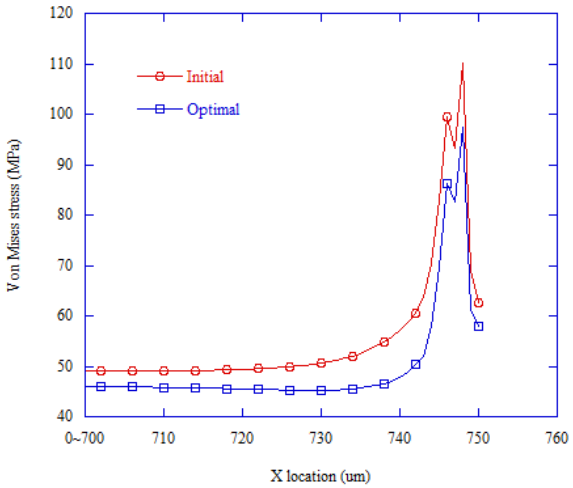
c. ILD layer



d. IMD layer



e. Aluminum layer f. USG layer



g. Silicon Nitride layer

Fig. 50: The residual stress following x-direction in different layer before and after optimization process

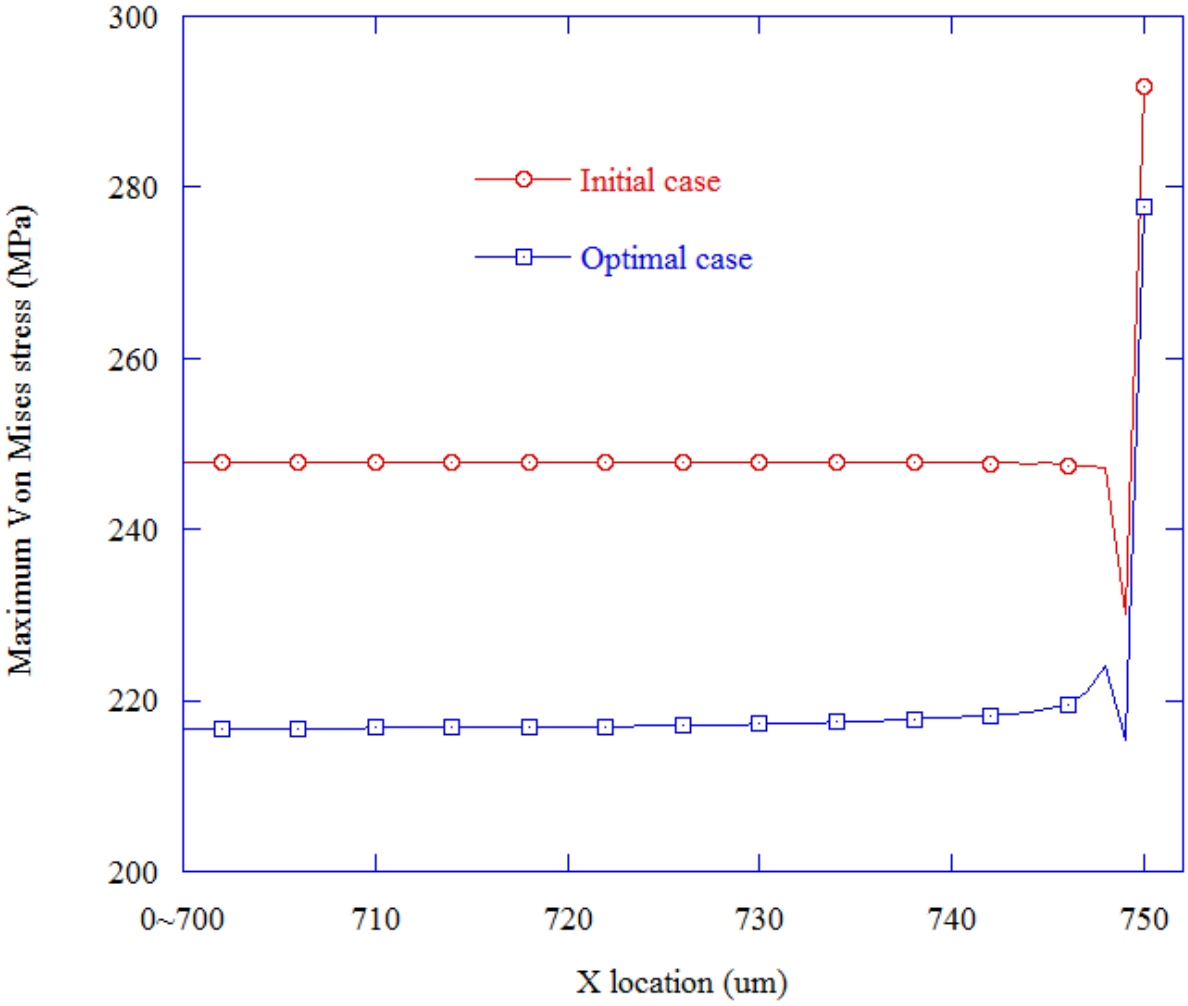
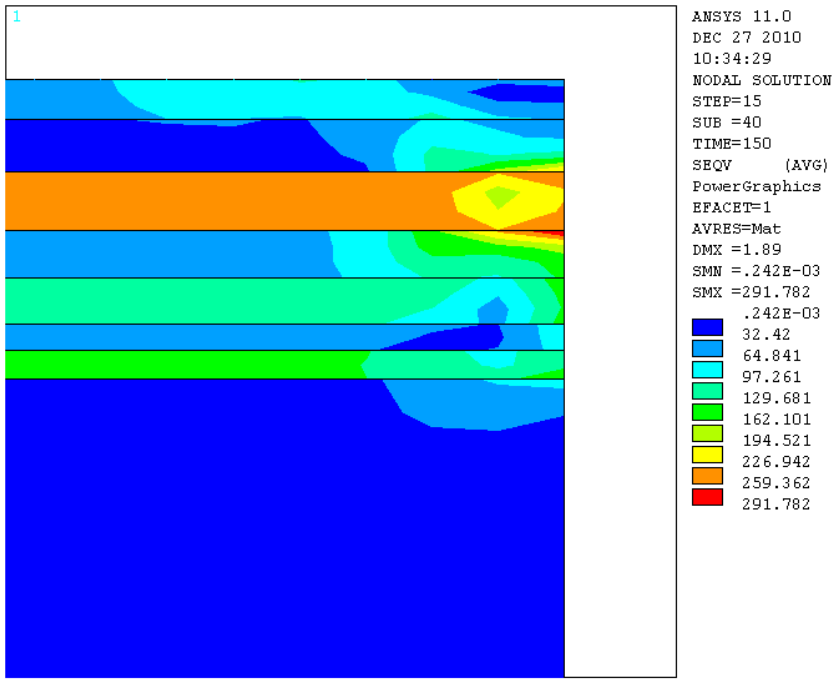
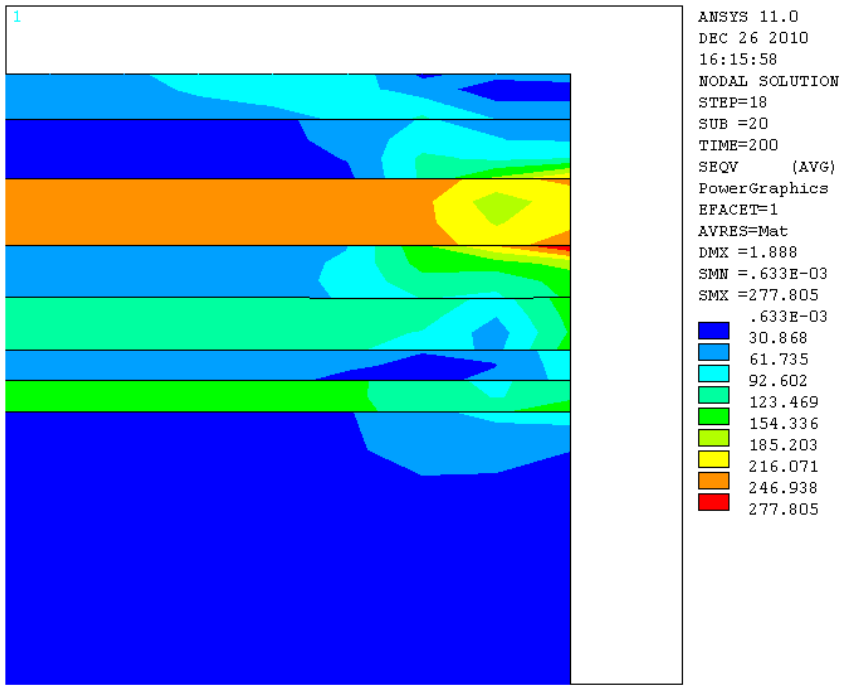


Fig. 51: The different maximum residual stress following x-direction before and after optimization process



a. Von Mises stress distribution in initial case



b. Von Mises stress distribution in optimal case

Fig. 52: The residual stress distribution in initial case and optimal case

4. CONCLUSION

Residual stress is of inherent importance in various respects in MEMS. The existence of the residual stress essentially changes the performance and reduces the structural integrity and longevity of MEMS devices. It may damage MEMS device during its fabrication and/or reduce its service life and also cause cracks in the film from the substrate. It's harmful for developing MEMS products. Therefore, understanding the residual stress characteristic and controlled it plays the important role in this research.

The present study includes two parts. First, the finite element simulation model is proposed to predict the pre-deformation caused by residual stress in CMOS-MEMS bridge structure. Through the finite element package, a finite element simulation model is developed in this prediction. Besides, the finite element simulation model is validated by the experiment according to the bridge structure fabricated MXIC 2P2M process. The residual stress inside the 2P2M bridge structure includes normal stress and gradients stress, the deformation is generated after the bridge structure released. Under that phenomenon, the load as the opposite residual stress is used to release the residual stress inside the 2P2M bridge structure and the deformation of the bridge structure can be observe in the simulation process. It finds that the simulation result agrees well with experimental data and the average deviation is suitable with the criteria. From this study, it can be concluded that the proposed method is an accurate, robust and efficient method to determine the pre-deformation caused by residual stress in MEMS through the bridge structure fabricated MXIC 2P2M process.

Secondly, the birth and death method is used to predict the residual stresses during the CMOS fabrication. The residual stress in the CMOS fabrication consists in the summation of the intrinsic stress and the thermal stress where the former is induced during the film – growth

process and the later is caused by the mismatch of coefficient of thermal expansion (CTE) between the films and the substrate. In this research, coupled heat transfer and elastic – plastic finite element stress analyses were combined to simulate the generation of thermal stresses during the CMOS fabrication process. The complicated physical fabrication process was idealized and a multiple layer by layer deposited structure was assumed. In the simulation, the geometry was updated layer by layer, the heat transfer and displacement is solved in the same time. Besides, the birth and death method that is used in this research is validated by verifying the numerical results with previous paper. This means that the proposed method can simulate the real model robust and effectively. On other hand, a simple method by cooling under room temperature was also proposed to effectively reduce the residual stress level in the CMOS fabrication with the possibility of reducing the residual stress.

The extend application of ANSYS combined with SCGM are used to minimize residual stresses in the CMOS fabrication process. The Von Mises stress is defined as object function to find the best valuable parameter in the fabrication process. The heat transfer coefficient and optimal temperature after complete deposition is choose as variable to reduce residual stress. After optimal process, the residual stress is reduced 14MPa and 4.8% percent. It means the suitable parameter fabrication can generate small residual stress in MEMS devices.

Finally, this present study proposes the methods which can provide the components to assist designer as a design reference and industrial development in the mass production process in MEMS field. In the other hand, the optimal residual stress in the CMOS fabrication can find the good parameter fabrication to improve the MEMS products and make knowledge about the residual stress in developing the fabrication process.

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